INSTRUCTION MANUAL

Models 361, 361 RM30

Counter-Timer

SERIAL NO. 1574

sophisticated

digital instrumentation

TRANSISTOR SPECIALTIES, INCORPORATED

PLAINVIEW, LONG ISLAND, NEW YORK

INSTRUCTION MANUAL

Models 361, 361 RM30

Counter-Timer

SERIAL NO. 1574

FOREWORD

This instruction manual describes Models 361 (Cabinet Model) and 361 R (Rack Model). These instruments are dual-channel counter/timer/frequency meters operating over the range from 0 to 2.5 megacycles.

UNPACKING AND INSTALLATION

PACKAGE

This counter was shipped to you in a scientifically designed packing complex, consisting of a set of accurately-fitted resilient pads, and a sturdy outer carton. Examine the carton for signs of external damage before proceeding to unpack. If external damage is discovered, notify the carrier before proceeding!

The top of the outer carton is marked as such. This surface should be carefully opened, to avoid penetrating the resilient pads. After the top is opened, remove the resilient pad at the top, exposing the handle of the instrument (in bench models) or the top of the dust-cover (rack-mounting models). The instrument may now be removed from the carton.

EXAMINATION

Next, examine the outside of the counter for any physical evidence of damage due to excessive shock and/or vibration, water leakage, etc. If the counter appears to be in perfect condition, you may proceed to install and operate it. If not, communicate with the carrier for instructions.

POWER SOURCE

Read the SPECIFICATIONS section to determine the input rating and requirements of this instrument. DO NOT PLUG THIS UNIT INTO A POWER LINE UNTIL YOU ARE CERTAIN THAT IT IS CORRECT IN NOMINAL VOLTAGE AND FREQUENCY. A stable power source of good waveform will yield best results, although the instrument will function over the entire rated range of input voltage and frequency.

AMBIENT TEMPERATURE

This instrument is rated (see SPECIFICATIONS section) for a certain MAXIMUM AMBIENT TEMPERATURE and this maximum must NEVER be exceeded, even during "standby" conditions, without consulting with our engineering department*, and obtaining written permission to do so. The minimum temperature rating must also be respected at all times.

The ambient temperature rating applies to the TEMPERATURE OF THE AIR SURROUNDING THE EQUIPMENT AND ENTERING THE COOLING PORTS. This is particularly significant in rack-mounting applications . . . remember that the air at the top of even a well-ventilated rack of dissipative equipment is usually at least 15°C higher than the external ambient! If in doubt, measure the ambient air with a thermometer located in the incoming air-stream at the cooling port.

SLIDES

It is important to remember, when installing slides on rack-mounted equipment, that the cooling ports must not be blocked. Consult our engineering department for assistance in applying the slide of your choice on this equipment.

SHIPPING BLOCK

Remove shipping block before using instrument. Failure to do so may cause overheating of instrument.

*This service is free, prompt, and very helpful. Many of our designs can be modified easily to operate at temperatures considerably in excess of maximum rating.

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	Gating Logic (609-D-191)	
	Signal Divider (609-D-195)	
	Decade Readout #22 (609-D-107)	
	Decade Readout #21 (609-D-106)	
	Time Base Generator (609-D-104)	
	Schematic Power Supply (620-C-132)	
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STANDARD WARRANTY

TRANSISTOR SPECIALTIES, INC., warrants to the original purchaser that equipment of its manufacture is free from defects in material and workmanship. This warranty is effective for a period of 2 years after delivery of the instrument to the original purchaser. Display tubes, semi-conductors, fuses, components, or accessories not so warranted by the original manufacturer are not warranted by Transistor Specialties, Inc.

Liability under this warranty is limited to servicing or adjusting any instrument returned to the Transistor Specialties, Inc., factory for that purpose, transportation charges prepaid, provided that investigation and factory inspection discloses that defect developed under normal and proper use and is covered by warranty terms. If defect is not covered by warranty terms, or has been caused by misuse or abnormal conditions, an estimated cost or repairs will be submitted to customer, and, upon his written authorization, repairs will be accomplished and billed at cost. Instruments will be returned with transportation charges collect.

This warranty is expressly in lieu of all other obligations or liabilities on the part of Transistor Specialties, Inc., and Transistor Specialties, Inc. neither assumes, nor authorizes any other person, including representatives of Transistor Specialties, Inc., to assume for them, any other liability in connection with the sale of Transistor Specialties, Inc. instruments.

MODEL 361
2.5 MEGACYCLE COUNTER-TIMER

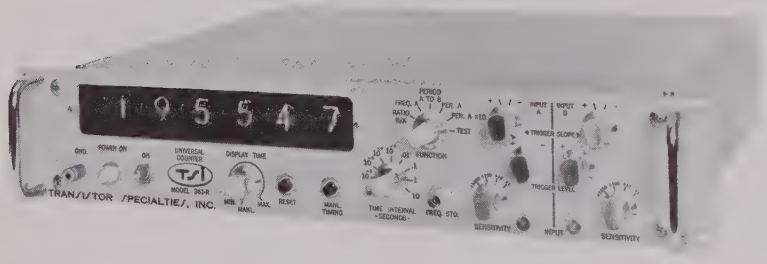
FEATURES:

ALL SOLID-STATE CONSTRUCTION-High reliability, low power drain.
IN-LINE NIXIE READOUT-six digits; instant, direct reading to 2.5 Mc.
HIGH ACCURACY-oven-stablilized crystal time base yields accuracy of ±1 count ±3 parts in 10^7/ week.
HIGHEST SENSITIVITY-Input amplifiers have 10 millivolt sensitivity, 1-megohm input impedance.
COMPACT-and completely self-contained. Rack and cabinet models available.

MEASURES:

FREQUENCY • PERIOD • TIME INTERVAL

FREQUENCY RATIO • PULSE WIDTH



DESCRIPTION:

The Model 361 is a truly-universal, precision counter-timer, containing every facility required for performing every conventional measurement in the time-frequency domain. No plug-in units, adaptors or attachments are required for the utilization of this versatile instrument in any of the following modes:

As an Event Counter: totalizing periodic or random events for the duration of any one of eight precise time intervals, or on a straight-count basis, to 999,999.

As a Frequency Meter: for measurement of pulse repetition up to 2,500,000 pps, and frequencies from 10 to 2,500,000 cps. Heavily-distorted waveforms are accepted without error.

As a Frequency Ratio Meter: to determine the ratio of pulses (or waves) occuring in one input channel to pulses (or waves) in a second input channel.

As a Time Interval Meter: measuring the time between the occurrence of two events from 1 microsecond to 10^7 seconds, as well as periodicity, and pulse width.

As a Secondary Frequency Standard: providing out-puts of 0.1, 1, 10 and 100 cycles, 1, 10 and 100 kilocycles, and 1 megacycle, accurate to ±3 parts in 10^7 per week.

The exceptional accuracy and stability of the Model 361 are derived from a thermally-stabilized oscillator which employs a low-drift 1 megacycle crystal. It can be easily checked against National Bureau of Standards station WWV and readjusted.

A self-checking feature permits testing every time base, using front panel controls. The six-digit inline Nixie readout requires no interpolation, is instantly readable in any ambient light.

The simple, logical panel layout permits use of the instrument by relatively inexperienced personnel, without error or confusion. A Function switch selects one of six operating modes: Ratio B/A, Frequency A, Period A/B, Period A, Period A X 10, and Test; a Time Interval switch selects one of eight intervals from 10 seconds to 10^{-6} seconds, or manual timing. Together, these controls provide an infinite variety of random-tally and time-frequency measurements. With appropriate transducers, parameters such as velocity, flow-rate and RPM can be measured.

361-0366

TRANSISTOR SPECIALTIES, INCORPORATED
120 TERMINAL DRIVE, PLAINVIEW, N.Y. 11803
PHONE (516) 935-8700

MODEL 361, 361-R

SPECIFICATIONS:

INPUT CHANNELS (A and B)

Range–	AC coupled, 10 cps to more than 2.5 Mc.
Sensitivity–	10 mv rms from 10 cps to 100 kc, 25 mv rms to 2.5 Mc. Absolute maximum input 150 v rms, 420 v peak to ground. (300 v dc peak blocking).
Impedance–	1 megohm, 40 pf shunt.
Trigger Level–	Adjustable front panel control. Trigger Slope selector switch.
Attenuator–	Four position, divide by: 1, 10, 100, 1000.
Trigger Error–	0.3% at 100 mv rms.

TIME BASE

Frequency–	1 Mc, oven stabilized.
Stability–	Long term, ±3 parts in 10^7 per week. Short term, ±1 part in 10^7 per 100 seconds.
Temperature–	0°C to 50°C, ±5 parts in 10^7.
Selection–	10^{-6} to 10 seconds selectable in decade steps. Manual position with push button for manual Time Base actuation.
Output–	Front panel BNC, 10^{-6} to 10 seconds as selected by front panel switch.

FUNCTIONS

Frequency A	10 cps to more than 2.5 Mc, accuracy ±1 count.
Period A and Period A x 10:	
Single Period	0 to 1 Mc.
Mult. Period	0 to 1 Mc.
Resolution	1 microsecond
Accuracy	$\pm 1 \text{ count} \pm \frac{\text{Trigger Error}}{\text{No. of per. avg.}}$
Period A to B, (Time Interval):	
Range	1 microsecond to 10^7 seconds. Standard frequency counted, 10^{-6} to 10 seconds in decade steps.
Ratio B/A:	
Range	Input A, 0 to 1.0 Mc. Input B, 0 to 2.5 Mc.
Accuracy	$\pm 1 \text{ count} \pm \frac{\text{Trigger Error}}{\text{No. of per. avg.}}$
Test	Self check: 1 μs to 100 ms counts 1 Mc. 1 second counts 100 kc. 10 seconds counts 10 kc.

DISPLAY TIME
0.2 to 10 seconds, continuously adjustable. Infinite in manual position.

OPERATIONAL TEMPERATURE RANGE
0-50°C

POWER REQUIREMENTS
35 watts (+8 watts peak oven power during heat cycle) at 115 or 230 v rms ±10% 50-400 cps nominal.

NOTE:

Model 364 and 364-R. . . . . .
Includes M15 and frequency extension to 5 Mc.

MECHANICAL SPECIFICATIONS
Model 361 (Cabinet)
8 3/4" high x 10 1/4" wide x 12 1/2" deep, 19 lbs. net, 25 lbs. shipped
Model 361-R (Rack)
3 1/2" high x 19" panel width x 16" behind panel, 17 1/2" deep overall, incl. panel elements. 20 lbs. net 30 lbs. shipped.

Front panel BNC connectors for Channel A, Channel B, and frequency Standard output. Rear Mounted BNC Connector for Gate Pulse output.

OPTIONS:

Consult factory for detailed descriptions,

M 7	External Electrical reset	$ 45.
M 8	Provision for use of external 1 Mc time base input. (Permits use of laboratory standard in place of internal oscillator).	$ 20.
M 9	External 1 Mc oscillator input. No internal oscillator. . . . . minus	$ 50.
M 10	Provisions for use of external 100 kc time base input. (External 100 KC, internal 1 Mc, switch selected)	$ 55.
M 15	Automatic decimal point. Also shows C, KC, MC or S, MS, μS	$100.
*M 21	Printer output, 1-2-4-8, '1' state neg. .	$150.
*M 22	Printer output, 1-2-4-8, '1' state pos. .	$150.
*M 25	Printer output, 1-2-2-4, '1' state neg. .	$150.
*M 26	Printer output, 1-2-2-4, '1' state pos. .	$150.
M 27	100 second time base in addition to existing time bases	$100.
M 30	Display storage. Provides continuous readout. All solid state circuitry for "hard" storage, no fading of numerals from one reading to the next Cost per digit	$ 15.
*M 46	Period multiplier permits period and multiple period average measurements to 10^7 periods. Includes a decade time base	$100.

Available on rack models only due to space limitations in the cabinet model.

PRICE:

6 digit model	$ 995.
5 digit model	$ 925.
4 digit model	$ 855.
364 and 364R 6 digits	$1490.

TSI
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III OPERATING INSTRUCTIONS

GENERAL

The APTI-METER is a dual-channel, digital-counting measuring instrument of laboratory quality. Its design makes it inherently capable of superior operation; however the potential of the instrument can be fully realized only if it is operated carefully and intelligently. The operator is therefore referred to Section IV, Theory of Operation, and Section V, Circuit Theory, so that he may become thoroughly familiar with the circuit effects of the operating controls. Prior to operation the APTI-METER should be checked as described in Section VII and adjusted if required as discussed in Section VI.

OPERATING CONTROLS

Figure 3-4, the final page of this section, illustrates and identifies the operating controls of the APTI-METER; the illustration may be folded out for ready reference in following the discussions below.

All operating controls are grouped logically on the front panel of the instrument upon which the control names and settings are clearly etched. The APTI-METER displays its measurements on a row of six NIXIE tubes appearing directly above the controls. Digits 1 through 9, and 0, may appear on each of the NIXIES; the display is, of course, self-luminous (orange colored) and is highly readable in any light. In addition to the controls proper, three BNC connectors and a pilot lamp are mounted on the panel. The lamp lights under "power-on" conditions. Input signals to Channel A are applied to the instrument via the BNC connector under the controls for that channel; Input signals to Channel B are applied via the BNC connector under the controls for Channel B.

Power Switch - This toggle switch applies full operating power to the APTI-METER. With the switch in the ON position the pilot lamp directly above will light.

Input Controls - The controls for Channels A and B are identical. Those for Channel A are grouped vertically under INPUT A; those for Channel B are similarly grouped under INPUT B. These controls will be described in order, from top to bottom, as they appear.

TRIGGER SLOPE - This control is a two-position switch with the positions marked "+" and "–" as shown in figure 3-4. In the "+" position, the channel with which the control is associated will respond only to positive-going signals. In the "–" position the channel will respond only to negative-going signals.

TRIGGER LEVEL - This control is a potentiometer which determines the base potential of a transistor in a voltage-selective amplifier. The control selects the triggering poin. on the input signal waveform. Operation of the TRIGGER LEVEL Control is discussed at some length below; it is extremely important to note here, however, that this control and the SENSITIVITY control interact and that the settings of each are critical to the extent that improper operation of either or both can result in false or inaccurate counting by the APTI-METER. Refer to " Adjustment of TRIGGER LEVEL and SENSITIVITY Controls" below. Maximum sensitivity is obtained only with proper setting of trigger level control.

SENSITIVITY Control - This control is a four-step attenuator. Through it use, the input signal is attenuated so that the attenuator output is divided by 1000, 100, 10, or 1. The switch positions reading from left to right are, accordingly: $\div 1000$, $\div 100$, $\div 10$, $\div 1$. This last ($\div 1$) represents a non-attenuated input and hence is the highest sensitivity setting of the instrument as $\div 1000$ is the lowest. As noted under TRIGGER LEVEL Control, above, improper setting of this control can result in false and/or inaccurate counting. It is important that this control be set to the lowest sensitivity position at which firm counting results. Refer to "Adjustment of TRIGGER LEVEL and SENSITIVITY Controls" below.

DISPLAY TIME Controls - These two controls consist of a two-position switch potentiometer and a push-button switch. The switch positions of the switch-potentiometer are called MANUAL and MIN-MAX. These controls determine the length of time that a display is retained on the NIXIE indicators after completion of a measurement. The potentiometer MIN to MAX setting is variable from 0.2 to 10 seconds. After the period selected, the instrument automatically clears to zero and repeats the measurement and display.

FUNCTION Control - This control is a six-position switch determining the mode of operation of the APTI-METER. The switch positions are labeled (from left to right): RATIO B/A; FREQ. A; PERIOD A TO B; PER. A; PER A X 10; and TEST. Table 3-1, Functional Modes and Control Settings, relates FUNCTION Control settings to operating modes and describes each mode.

TIME INTERVAL Controls - This control group consists of a nine-position switch and a push button switch. The nine-position switch establishes precisely the time interval during which measurement(s) of the input signal(s) will be performed. The M position switches control of the interval to the MANUAL TIMING pushbutton where the interval is started by depressing the pushbutton and is terminated by depressing the pushbutton a second time. The selected intervals may be (left to right): M, 10^{-6}, 10^{-5}, 10^{-4}, 10^{-3}, .01, .1, 1, and 10 seconds.

FREQ. STD. - This BNC connector makes the internally generated one-megacycle as well as 100 KC, 10 KC, 1 KC, 100, 10, and 0.1 cps timing signals available for external use a highly-accurate, highly-stable clock or frequency standard.

ADJUSTMENT OF TRIGGER LEVEL AND SENSITIVITY CONTROLS

INPUT SIGNAL CONSIDERATIONS

The APTI-METER is an unusally versatile instrument, designed for use with a wide variety of waveshapes, over a very broad frequency range. Because of this versatility, and because of its inherent sensitivity and precision, the APTI-METER requires careful application and adjustment, if inaccurate or erroneous measurements are to be avoided.

To insure reliable counting and measurement, it is highly desirable that the nature of the input signal be known; if it is not known, and if an oscilloscope is unavailable, it is possible to perform measurements of the signal, but the results are subject to question even though they appear to be consistent. For example, if it is known that the signal is a uniform, symmetrical sine wave or square wave, we can be sure that once the instrument controls are properly adjusted, the unit is being triggered properly once each cycle, and that the numerical display on the Nixie indicators is a reliable measurement. However, Figure 3-1 illustrates the ambiguity that can result if we conveniently assume that the signal is a uniform symmetrical wave and it is not.

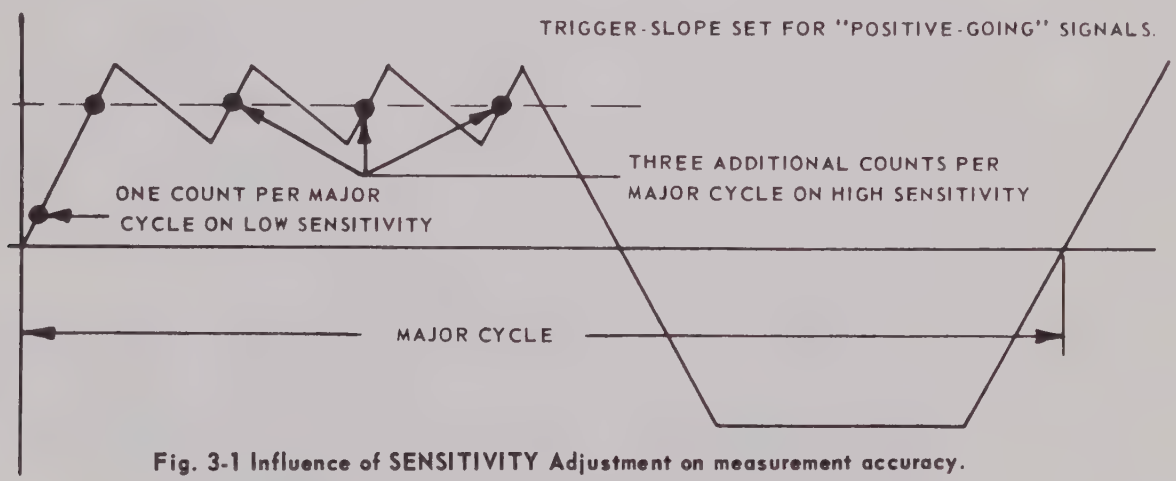

TRIGGER-SLOPE SET FOR "POSITIVE-GOING" SIGNALS.
THREE ADDITIONAL COUNTS PER MAJOR CYCLE ON HIGH SENSITIVITY
ONE COUNT PER MAJOR CYCLE ON LOW SENSITIVITY
MAJOR CYCLE

Fig. 3-1 Influence of SENSITIVITY Adjustment on measurement accuracy.

The illustration shows that under one condition of sensitivity adjustment the unit will be triggered once for each major cycle, and the display will give an accurate count, while another sensitivity setting will produce four counts per major cycle, and the display will be in error by a factor of 4 to 1. The additional triggering points shown in Figure 3-1 could be integral parts of the signal under measurement, or could be random noise impulses generated by a defective component or circuit in the signal source; in either case, adjustment of the APTI-METER sensitivity to a suitably low value would avoid the false triggering, while permitting the true signal to trigger the instrument consistently.

Figure 3-2 illustrates another difficulty that is avoided when the nature of the input signal is known. The trigger circuit in the APTI-METER input channel is influenced by the average value of the amplified signal. For symmetrical input signals (such as a sine wave) the average value of the signal is zero; but when the signal is assymetrical with respect to the base line (ground), and particularly when the assymetry is extreme, the trigger circuit may be "blocked" by the resulting high average (DC) value of the amplified waveform. Proper adjustment of the TRIGGER LEVEL control inserts an appropriate offset bias in series with the amplified signal to "unblock" the trigger circuit. Figure 3-2 illustrates this situation.

Low-Level Signals must be carefully accommodated to avoid loss of instrument accuracy. Ground-loop anomalies, especially those due to ground currents circulating in the shields, are particularly significant at these levels. For this reason, every effort should be made to insure that:

1. Only one point in the system is grounded.
2. A good ground is used.
3. All paths for circulating currents are rerouted so as to prevent their flowing through the cables connected to the APTI-METER.

The Instrument is sufficiently sensitive that it may be influenced by very strong electro-magnetic or electrostatic fields. Such fields should be avoided, contained by shielding, or deflected from the instrument and its leads.

TRIGGER LEVEL Control Adjustment - This control is continuously variable and is used to select that level on the input waveform where firm triggering results. As may be seen below, either channel may be adjusted to respond to either a positive-going or negative-going waveform (See TRIGGER SLOPE Control discussion in this section and also figure 3-2.). The TRIGGER LEVEL Control is properly set so as to select a triggering point on a portion of the waveform which is uncluttered by adjacent variations that might produce spurious triggering,

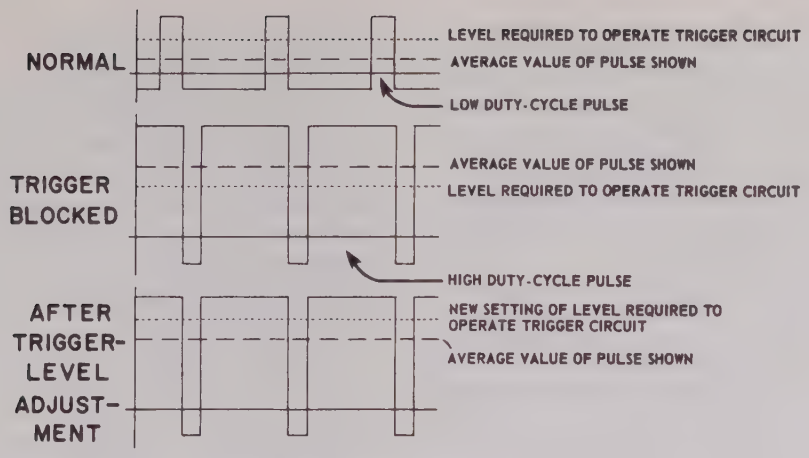

NORMAL
LEVEL REQUIRED TO OPERATE TRIGGER CIRCUIT
AVERAGE VALUE OF PULSE SHOWN
LOW DUTY-CYCLE PULSE
TRIGGER BLOCKED
AVERAGE VALUE OF PULSE SHOWN
LEVEL REQUIRED TO OPERATE TRIGGER CIRCUIT
HIGH DUTY-CYCLE PULSE
AFTER TRIGGER-LEVEL ADJUST-MENT
NEW SETTING OF LEVEL REQUIRED TO OPERATE TRIGGER CIRCUIT
AVERAGE VALUE OF PULSE SHOWN

Fig. 3-2 Use of TRIGGER LEVEL adjustment to prevent block by pulses with extreme duty cycles.

and should be at that point where rate of change is maximum. The "+" and "–" positions of the TRIGGER SLOPE Controls determine whether the APTI-METER will operate on positive-going only or negative-going only voltage excursions. Provided that the SENSITIVITY SWITCH and TRIGGER LEVEL Control are properly set, a pulse is produced as a result of the arrival of the instantaneous voltage (attenuated by the SENSITIVITY SWITCH – controlled attenuator) at the voltage level selected by the TRIGGER LEVEL Control. Figure 3-3 illustrates this:

When the TRIGGER LEVEL index is vertical, the level is set approximately midway in the range. In this position the "Schmitt Trigger" circuit will generate a sharp pulse each time the input signal passes through the trigger level voltage. This is the proper setting for symmetrical periodic inputs. However, for asymmetrical inputs, setting of the TRIGGER LEVEL Control at the proper setting must be determined by a slow rotation of the control to the mid-point between the positive and negative extremes of the waveform. These extremes may be detected by a total or marginal failure to trigger. This last is mani-

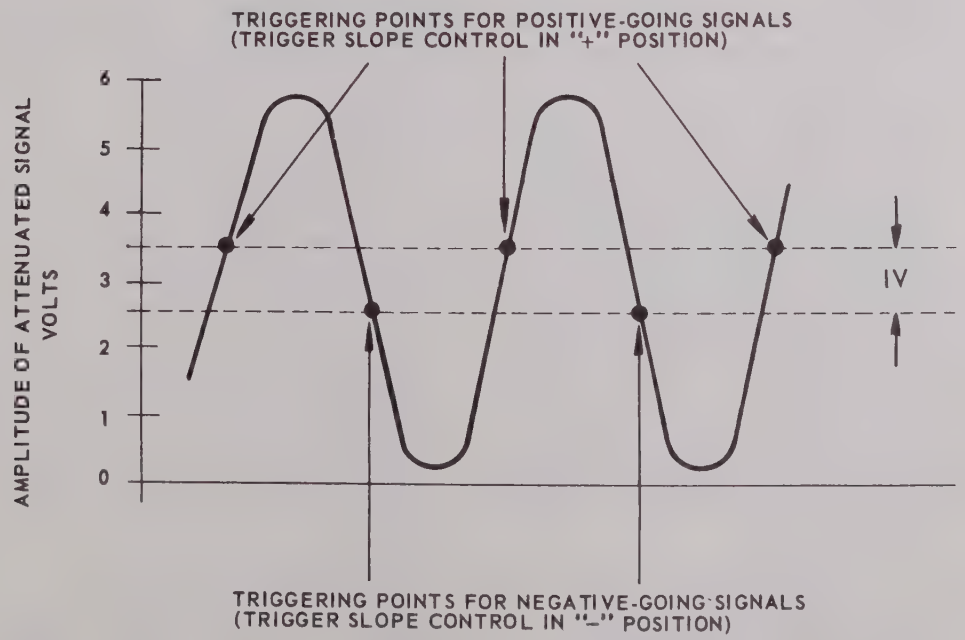


Fig. 3-3 Effect of TRIGGER SLOPE Settings

fested on Channel A by a NIXIE display of O's or by irregular counting, and on Channel B by nixies "running wild". It is obvious that wherever possible the shape, amplitude, and frequency of the input waveform should be determined. This is needed particularly in the case of aperiodic inputs, to permit greatly simplified TRIGGER LEVEL and SENSITIVITY SWITCH setting adjustments.

SENSITIVITY CONTROL ADJUSTMENT

This control is a four-step attenuator used to select the desired gain setting of the amplifier circuit. The four settings, reading clockwise are: ÷ 1000, ÷ 100, ÷ 10, and ÷ 1. As discussed below, the proper setting of the SENSITIVITY SWITCH is at the lowest sensitivity position which produces reliable counting. Sensitivity increases in a clockwise direction; the ÷ 1 position is highest sensitivity, ÷ 1000 the lowest. The optimum setting is determined by the RMS value of the input signal and should be such as to attenuate the input signal to a value of 50 to 100 mv approximately. For example, a 6V RMS input signal will be attenuated to 60MV RMS , with the SENSITIVITY SWITCH AT ÷ 100. Attenuated signal values between 50 and 100MV RMS will, in most measurements, provide firm and reliable counting.

Too high a setting of the SENSITIVITY SWITCH may result in saturation of the following amplifier, distorting the waveform through the pulse forming network and producing unreliable counting. Too low a setting of the sensitivity switch may result in weak signals being "missed" and hence an improper count.

SEQUENCE OF OPERATION

Initial Connections

a. Connect the APTI-METER power cable to 115 volt, 60 or 400-cycle power line, and turn the front panel POWER switch to the ON position. The POWER ON pilot lamp should light.

b. Allow at least two minutes for the instrument to warm up; ignore random behavior of the Nixie display during this interval. If the ultimate accuracy is required, and particularly if the instrument has been stored at a low ambient temperature, a 30-minute warm-up interval is recommended, to permit the crystal oven to reach thermal equilibrium.

c. Set the two SENSITIVITY controls to the proper lowest position (See previous discussion) and connect the input signals to the A and B input-channel BNC connectors, via appropriate leads. When only a single input is used, this should be applied to channel A.

CAUTION

Note that the input channels have a common (chassis) ground. Be sure to respect the maximum ratings specified for the input circuits (200 VDC in the X1 position of the attenuator, and 420 V peak instantaneous in the X1000 position).

FUNCTIONAL MODES

ACTIONS PER TIME INTERVAL

This mode is used for determining the total number of events (random or periodic) occuring during any selected time interval between 10 seconds and 10 microseconds.

1) Turn power ON; allow instrument to warm-up.
2) Connect the input signal to channel A.
3) Set the FUNCTION selector to FREQ. A.
4) Adjust the DISPLAY TIME control to the desired period (0.2 to 10 seconds is the adjustment range). In MANUAL position, the display is held indefinitely until cleared by actuating the MANUAL RESET Button.
5) Set the TIME INTERVAL switch to the appropriate interval.
6) Refer to discussion in previous subsection for procedures used to ensure consistent triggering by the input signal, and set TRIGGER LEVEL and SENSITIVITY controls accordingly.

STRAIGHT COUNT

This mode is used to count pulses or sine waves without limit (fed to channel A) between two successive operations of the MANUAL TIMING button.

The procedure is identical to that described above for ACTIONS PER TIME INTERVAL, except the TIME INTERVAL selector is set to "M". The MANUAL TIMING pushbutton is pressed once to initiate the time interval, and the instrument counts continuously until the pushbutton is pressed a second time to terminate the interval. Counting range: up to 999,999.

FREQUENCY A

Identical to ACTIONS PER TIME INTERVAL. By setting the TIME INTERVAL selector to 1 (second), the display will read directly in cycles-per-second. (0.1 to 1,000,000 cps), or pulses per second (0 to 1,000,000 pps).

PERIOD A

This mode is used to measure the interval between two successive input pulses, or between successive cycles of a periodic-waveform, fed to channel A. Particularly useful for accurate low-frequency determination. With power ON:

1) Connect the input signal to Channel A.
2) Set the FUNCTION selector to PER A.
3) Set the TIME INTERVAL selector to the appropriate interval.* This determines the number of internal timing pulses generated per second (0.1 to 1,000,000). The first incoming signal pulse initiates a count of these timing pulses, the second signal pulse terminates the count, and total is displayed on the Nixie indicators.)
4) Set INPUT A controls (TRIGGER LEVEL, SENSITIVITY) as required by input signal.
5) Adjust the DISPLAY TIME control to the desired period (0.2 to 10 seconds is the adjustment range). In MANUAL position, the display is held indefinitely until cleared by actuating the MANUAL RESET button.

*Use position 10^{-6}, normally, for most precision time-interval measurements.

PERIOD A X 10

This mode provides a 10-cycle average period measurement for comparison with a PERIOD measurement. It counts the internally-generated timing pulses occuring between the first and eleventh input pulses (or cycles of a periodic waveform) on channel A. With power ON:

1) Set the FUNCTION selector to PER. A X 10; other procedures remain same as described for PERIOD A above. Divide the total count displayed by 10, to obtain an average time interval for one period.

PERIOD A-B

PERIOD A-B measurement (or any time-interval measurement which uses both channels) depends upon the proper relationship of the TRIGGER LEVEL Control, TRIGGER SLOPE control, and SENSITIVITY SWITCH settings for each channel. After the proper SENSITIVITY SWITCH settings for both channels have been made, the A TRIGGER LEVEL Control should be set to the mid-position between the positive and negative extremes of the waveform. Again, these extremes are detected by a total or marginal failure to trigger as shown by the NIXIES display of O's or irregular counting.

If reliable triggering is not quickly achieved by setting the A TRIGGER LEVEL control to its mid-point, the SENSITIVITY SWITCH may be set at too low a level. In this case sensitivity should be increased and the TRIGGER LEVEL setting procedure repeated.

After the channel A SENSITIVITY SWITCH and TRIGGER LEVEL settings have been made, the channel B SENSITIVITY SWITCH and TRIGGER LEVEL may be set. With the SENSITIVITY SWITCH at an appropriate setting (determined by characteristics of the signal input) find the extremes of the pulse as discussed above by a rotation of the TRIGGER LEVEL control, and set the B TRIGGER LEVEL control to the mid-point between them. If Channel B fails to trigger, the NIXIE display will "run wild" until the B TRIGGER LEVEL control is at a setting which permits effective triggering. It is important to understand that proper triggering action depends upon proper settings of both the SENSITIVITY SWITCH and the TRIGGER LEVEL CONTROL. Proceed as follows:

1) Turn power ON
2) Connect "Start" input signal to Channel A and "Stop" signal to Channel B.
3) Set FUNCTION control to PERIOD A-B.
4) Set A TRIGGER SLOPE TO "+" and B TRIGGER SLOPE to "–".*
5) Set SENSITIVITY and TRIGGER LEVEL controls as discussed previously, observing precautions.
6) Set DISPLAY TIME to desired display period.
7) Set TIME INTERVAL to time over which period is to be measured. See * under PERIOD A discussion above.

RATIO B TO A

In this mode the instrument counts pulses (or cycles) of the signal on Channel B between successive pulses (or cycles) fed to Channel A. This procedure is the same as inserting an external time-base on Channel A and counting on Channel B. With power ON:

1) Connect the lower frequency input signal to Channel A the higher-frequency signal to Channel B.
2) Set the FUNCTION selector to RATIO B/A.
3) The TIME INTERVAL selector is inoperative in this mode, and can be left in any position.
4) Adjust the DISPLAY TIME control to the desired period (0.2 to 10 seconds is the adjustment range. In MANUAL position, the Nixie display is held indefinitely, until the MANUAL RESET button is pressed).
5) Refer to previous ADJUSTMENT OF TRIGGER LEVEL AND SENSITIVITY CONTROLS, for procedures used to adjust these controls.

SELF CHECKING

This mode is used to make a periodic check of the APTIMETER accuracy. The output of the internal clock is fed to the input of Channel A, and the count interval is selected by means of the TIME INTERVAL control. A check of the NIXIE display reading for each of the 8 settings of the control reveals the accuracy of each. See procedures in Section VII, SERVICING.

1) Set the FUNCTION selector to TEST.
2) Set the DISPLAY TIME control (see step 4 above).
3) Rotate the TIME INTERVAL control through the successive positions from 10 to 10^{-6}, checking the count on the Nixie display, for each interval. Refer to Section VII for Nixie displays corresponding to switch settings.

*In the Period A–B mode the Channel A TRIGGER SLOPE selects the polarity of the voltage excursion which starts the timing period, and the Channel B TRIGGER SLOPE selects the polarity of the voltage excursion which stops the timing period. Therefore:

When measuring the width of a positive-going pulse, set Channel A TRIGGER SLOPE to "+" and Channel B TRIGGER SLOPE to "–."

When measuring the width of a negative-going pulse, set Channel A TRIGGER SLOPE to "–" and B to "+."

FUNCTIONAL MODES AND CONTROL SETTINGS

This chart describes the front-panel adjustments necessary to obtain each of the functional modes provided by this instrument. It is suggested that the operator read the THEORY OF OPERATION section for a logical description of the internal behavior of the instrument in each mode.

MEASUREMENT	CONTROL SETTINGS			INPUT TO:		FUNCTION
MODE	FUNCTION SELECTOR	TIME INTERVAL SELECTOR	DISPLAY TIME CONTROL	CHANNEL A	CHANNEL B	DESCRIPTION
ACTIONS PER TIME INTERVAL	FREQ. A	10^{-6} to 10	any (NOTE 1)	signals to be counted	none	Totalizes random or periodic events occurring in any selected time interval. NOTE 2
STRAIGHT COUNT 0-999,999	FREQ. A	M	any (NOTE 1)	signals to be counted	none	Counts pulses or sine-waves fed to channel A without limit between 2 successive operations of the MANUAL TIMING PUSHBUTTON.
FREQUENCY 0.1 cps – 1 megacycle/sec. 0-1 million pps	FREQ. A	10^{-6} to 10	any (NOTE 1)	signals to be counted	none	Counts pulses or cycles fed to channel A during the selected time interval. By setting to 1 second interval, reads directly in cps or pps. NOTE 2
PERIOD A (particularly useful for accurate determinations of low frequencies)	PER. A	10^{-6} to 10 (NOTE 3)	any (NOTE 1)	signal(s) denoting beginning and end of period.	none	Internally-generated timing pulses are counted between successive input pulses (or between successive cycles of a periodic waveform) fed to channel A. NOTE 2
PERIOD A x 10 (yields 10-cycle average information, to be compared with above 1-cycle data) Gives greater accuracy in period measurements	PER. A x 10	10^{-6} to 10 (NOTE 3)	any (NOTE 1)	signal(s) denoting beginning and end of period.	none	Internally-generated timing pulses are counted between the first and eleventh pulse (or cycle of a periodic waveform) fed to channel A. Total counted is then divided by 10 to determine average for one pulse interval cycle. NOTE 2
PERIOD A – B (permits phase-angle, pulse-width, and synchronizing measurements, and timing of relays, shutters, etc. Velocity, ballistics, and viscosity determinations may be made to very high accuracies.)	PERIOD A to B	10^{-6} to 10 (NOTE 3)	any (NOTE 1)	signal denoting beginning of period	signal denoting end of period	Internally-generated pulses are counted during the interval between a signal fed to channel A and a signal fed to channel B. NOTE 2
RATIO B/A Effectively same as inserting external time-base on Channel A and counting on Channel B.	RATIO B/A	any	any (NOTE 1)	lower-freq. signal	higher freq. signal	Input B is counted during the time interval between successive pulses (or cycles) fed channel A.
SELF-CHECKING (also useful as digital "clock")	TEST	10^{-6} to 10	any (NOTE 1)	none	none	The output of the clock is internally fed channel A, and count interval is selected by setting Time Interval Knob. Thus the instrument may be checked at each of 8 settings.

NOTE 1. Display is retained for period of time selected on "display time" control (0.2 – 10 seconds) after which instrument clears to zero and repeats measurement. Display may be held indefinitely (and manually cleared by means of the "reset" button) by setting "display time" control to "MANUAL".

NOTE 2. A gating pulse is generated during the "count" interval. This pulse is approximately rectangular, 5V amplitude, positive polarity, quiescent value approximately –5V, direct coupled.

NOTE 3. This time-duration range corresponds to timing-pulse frequencies from 1 megacycle/sec. to 0.1 cycles/sec, internally generated to crystal accuracy of ± 3 parts in 10^7.

IV THEORY OF OPERATION

Before attempting a detailed analysis of the schematic diagram of this instrument, let us turn our attention to a group of block diagrams which describe the instrument functionally, and then to a number of simplified schematics of individual circuits in the various blocks.

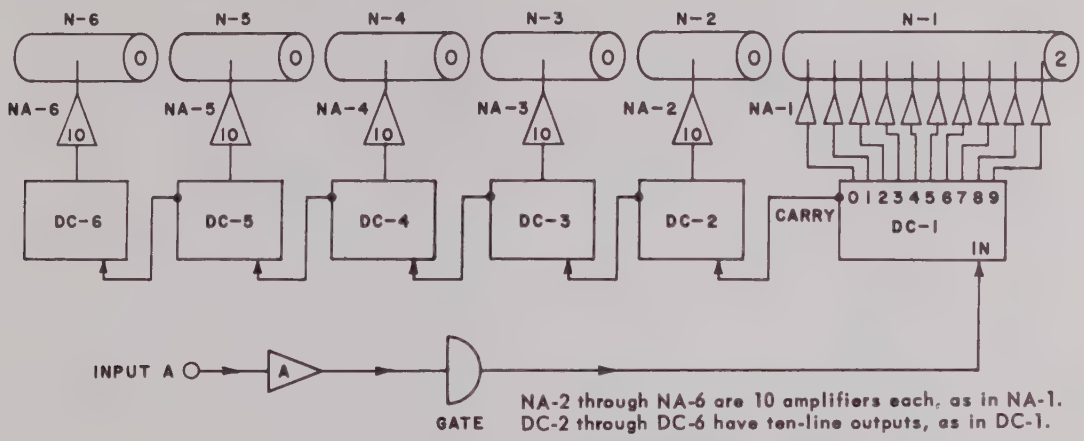


Fig. 4-1 Simplified Block Diagram #1: "STRAIGHT COUNT"

STRAIGHT COUNT (Refer to Figure 4-1)

The simplest and most basic function of this instrument is its use as a straightforward unlimited counter, as in the "STRAIGHT COUNT" mode described earlier. Pulses or other varying voltage signals, periodic or aperiodic, are fed into input A. The signals are amplified, limited, and shaped into pulses suitable for excitation of the first decade counter, and are gated into that counter (DC-1).

For the purposes of this functional description, let us define a decade counter. This useful circuit has two input terminals and eleven output terminals. Ten of the output terminals correspond to the "states" (conditions) of the counter:

"0" corresponds to the condition in which the circuit has not received an input pulse since being "cleared" (emptied).

"1" corresponds to the condition in which the circuit has received one input pulse since being "cleared".

"2" corresponds to the condition in which the circuit has received two input pulses since being cleared... etc.

In each state, the output terminal corresponding to that state will be at a positive voltage level, while all of the other nine terminals will be at a negative voltage level.

The eleventh output terminal is the carry terminal. This terminal produces a short positive pulse during the interval when the decade counter is transferring from the "9" state back to the "0" state, in response to the tenth pulse fed into it since it was cleared. Thus, the time sequence of outputs occuring on all eleven lines for the first 11 pulses is as shown in the chart below:

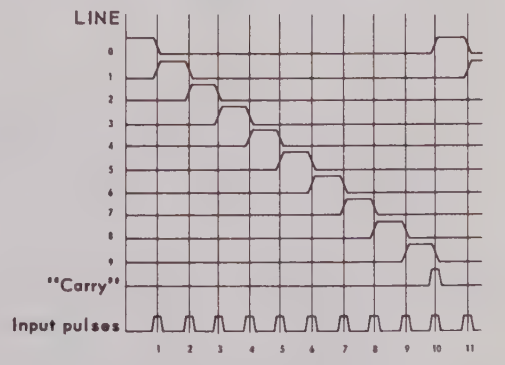


Fig. 4-2 Output Time Sequence

The signals to be counted are fed into one of the two input terminals. The other input terminal is the "clear", or "reset to zero" terminal. A positive signal pulse fed to this terminal will force the decade counter to the "0" state, "emptying" it of any residual count information it may have acquired previously.

Each of the ten "states" of the first decade counter (DC-1) results in a signal fed to one of the first group of ten nixie amplifiers (A-1). This signal results in the excitation of the appropriate electrode on the first nixie tube (N-1) displaying the appropriate number — that is, the number corresponding to that state of the counter.

Before the process of counting is begun, all decade counters have been forced to their "zero" state by a common "clear" signal. Thus before counting begins, all nixies display "0", and the total display is:

"000000"

As pulses are fed to the first decade counter, it "steps" from state to state, causing the first nixie tube to display 1,2,3, . . . etc., in turn, until "9" is reached. At this point, the first decade has reached its capacity. Upon receipt of the next pulse, the counter returns to state "0", and feeds a "carry" pulse to the second decade counter, DC-2. Such a "carry" pulse is generated by each of the decade counters (except DC-6) during the transition from "9" state to the "0" state.

The second decade counter (DC-2) steps from "0" to "1" when it receives the first carry pulse from DC-1. This change in state results in a display of "1" on N-2, the second nixie tube, which, when read in conjunction with the "0" state of N-1, reads "10", which is appropriate, since it was the tenth pulse that caused the "carry".

It should be noted that the total display reads:

"000010"

since all other nixie tubes (N3 through N6) reflect the zero-states in DC-3 through DC-6.

For future reference, it should be noted that the first decade counter and its associated readout circuitry is referred to as the "units" decade, the next array is referred to as the "tens" decade, the next as the "hundreds" decade, etc., through the sixth, which is called the "hundred-thousands" decade.

PERIOD MEASUREMENT

In this mode of operation, an externally-generated time interval is measured by counting the number of pulses of an internal generator occuring between the beginning and the end of the interval. The internal generator is extremely stable, and its frequency is set very precisely.

Let us assume that the beginning and end of the time interval to be measured are marked by two successive pulses fed to input A.

In the block diagram of Figure 4-3, the first pulse "opens" a gate circuit, permitting pulses produced by the internal generator to be fed to DC-1, the first decade counter. The second successive pulse on input A "closes" the gate circuit, halting the flow of pulses into the counter. The total count displayed on the Nixies, divided by the frequency of the internal generator, which is known, yields the time interval between the two pulses, directly in seconds. If, for example, the internal generator is producting pulses at the rate of 1 million per second, and the total count at the end of the period measurement is 560, 043, the time interval measured was 0.56043 seconds, to the accuracy of the counter and the internal generator. If the internal generator is stable (and accurately known) to ±1 part in a million, and the counter is accurate to ±1 count, then the total possible error in the observed time interval is less than ±2 microseconds.

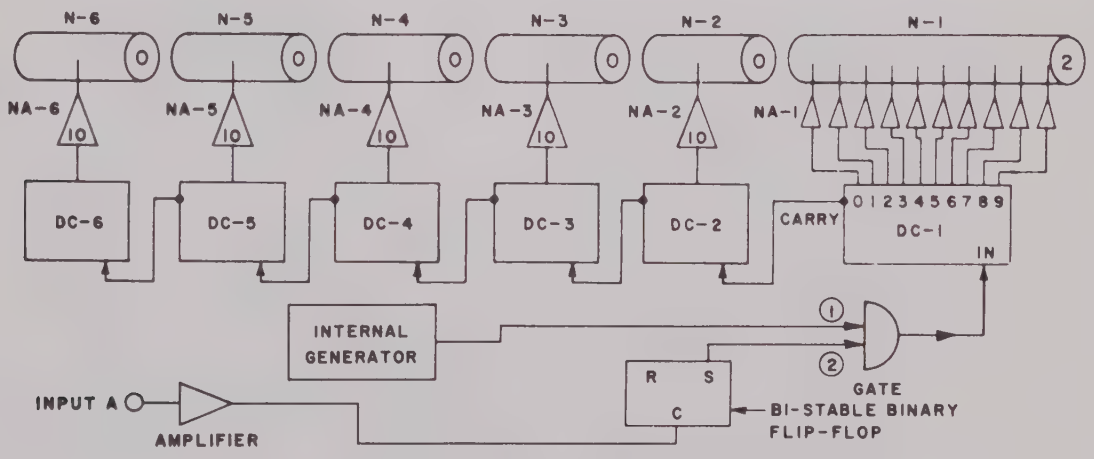


Fig. 4-3 Simplified Block Diagram #2 – Period Measurement

As the counting process continues, a carry pulse is fed To DC-2 every time DC-1 reaches capacity and passes from "9" back to "0". Eventually, DC-2 reaches capacity, and, on the next carry pulse it receives, generates a carry pulse of its own, which is fed to DC-3. This occurs on the 100th input pulse.

The process may continue until the total capacity of the counter has been used: 999,999 counts. The one-millionth count clears the counter back to zero.

Let us now examine the mechanism by which the gate circuit functions. This circuit has two input terminals and one output terminal. For the purposes of this functional discussion, let us assume that all signal pulses are positive in polarity. We may then describe the behavior of the gate circuit as follows:

> An output pulse appears when, and only when, signal pulses simultaneously exist on both input #1 and input #2. This kind of gate is called an "AND" gate. It is one of the basic logical building blocks

of all digital circuitry. Since one of the input lines is fed positive pulses from the internal generator, and the other is fed the output of the flip-flop circuit, we can say that the gate is "open" when, and only when, the output of the flip-flop circuit is positive.

The graph below illustrates the behavior of an AND gate.

Another basic logical building block employed in this kind of digital circuitry is the bistable binary flip-flop. For the purposes of this functional description, let us describe this circuit as one which, when it receives sucessive positive pulses on its input line, causes its output terminal to switch from a positive voltage level to a negative voltage level, and back to the positive level, alternating in polarity in response to the succession of input pulses. Actually, a flip-flop makes available two complementary output terminals, one of which is positive when the other is negative, and vice versa. One usually assigns a (purely arbitrary) nomenclature to the two possible output sets, as follows:

A particular output terminal is designated as the set terminal, and the other is designated as the reset terminal. Thus the flip-flop is said to be "set" when its set terminal is positive, and "reset" when its reset terminal is positive.

In Figure 4-3, we employ only one of the two output terminals of the flip-flop shown, and we feed its input terminal from the channel A amplifier, which receives the successive pulses on input A. The first pulse on input A, appropriately shaped and amplified, sets the flip-flop so as to open the gate. The second pulse resets the flip-flop, closing the gate.

Many variations of the basic period measurement described above are provided for in this instrument. In the simplest one, called "PERIOD A x 10", provision is made for the insertion of a decade counter stage between the amplifier and the flip-flop. The "carry pulse" output of the counter is fed to the input of the flip-flop. Thus, one input pulse is fed to the flip-flop for every 10 pulses fed to input A. The period measurement made in this mode is, then, the period between a particular pulse and the eleventh succeeding input pulse.

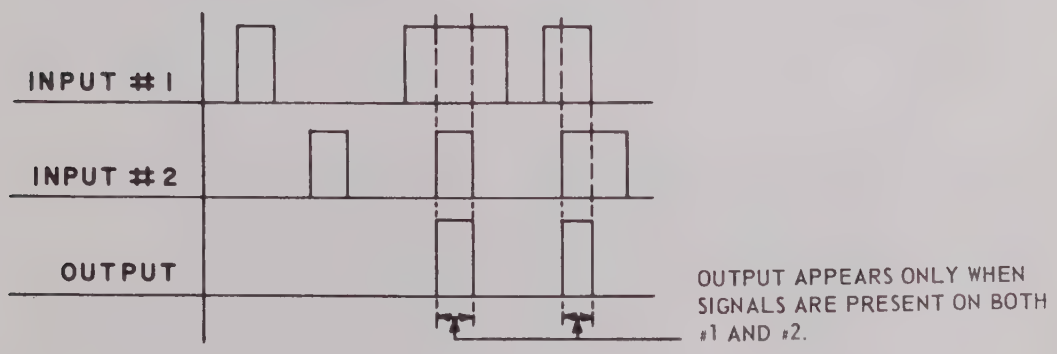


Fig. 4-4 AND Gate Operation

Another useful mode of period measurement is "PERIOD A-B". This mode is shown in the simplified block diagram figure 4-5.

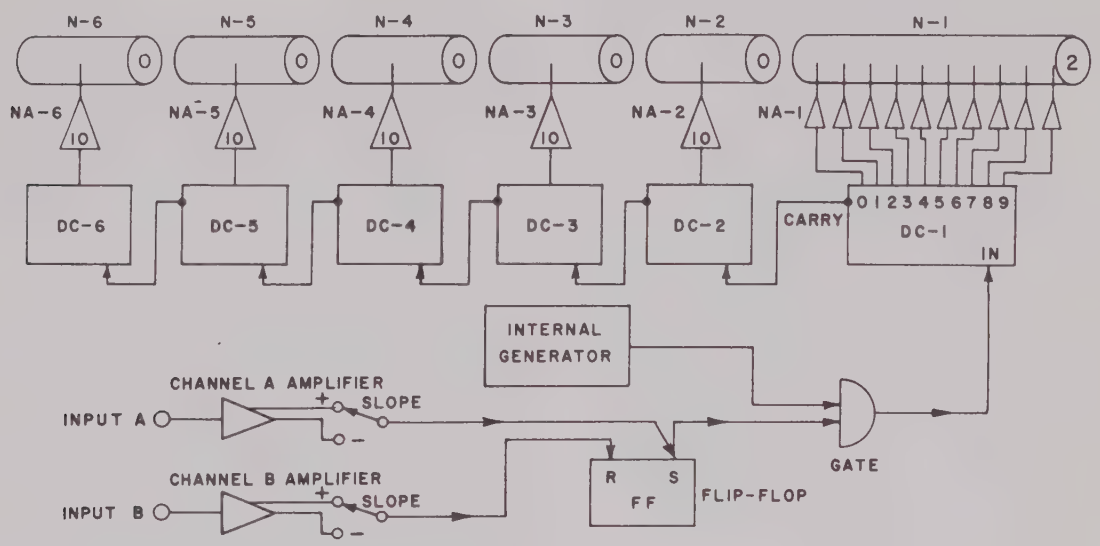


Fig. 4-5 Simplified Block Diagram #3 – Period A-B Measurement

In order to understand the behavior of this mode, it is necessary to amplify our description of the basic flip-flops employed in this instrument. It must be appreciated that the state of the flip-flop may be changed in three ways:

1. By feeding a pulse to what we have called the "input" terminal. This pulse "complements" the flip-flop — that is it changes its state from whatever existed before the pulse arrived to the opposite or complementary state. If the flip-flop was "set" before the pulse arrived it is "reset" by the pulse and, if it was "reset" before the pulse arrived, it is "set" by the pulse.
2. The state of the flip-flop may also be changed by feeding a sufficiently large pulse of sufficiently long duration to the reset terminal, the pulse polarity being such as to reverse the state of that terminal. In other words, if the reset terminal is at a negative voltage level, a positive pulse fed to that terminal will cause the reset terminal to go positive and stay positive, "resetting" the flip-flop.
3. The same reversing effect may be obtained by feed-in a sufficiently large pulse of appropriate polarity and sufficiently long duration to the set terminal. Either polarity condition may be reversed at either output terminal, by feeding that terminal with a pulse of opposite polarity and sufficient amplitude and duration.

With this additional information, it is now obvious that, after an input pulse fed to channel A has been used (as before) to set the flip-flop (opening the gate and starting the counting process) an input on Channel B can be used to reset that same flip-flop, stopping the counting process The reset action is performed at the reset output of the flip-flop. In this mode, then, the period measured is that which occurs between a pulse on input A and the next successive pulse on input B.

It should be noted that each of the amplifiers is equipped with a selector switch, permitting it to discriminate between positive-going and negative-going signal slopes, and permitting the use of either polarity slope as its input signal. This feature not only adds to the general flexibility of the counter, but it specifically implements certain very useful variations of the "PERIOD A-B" mode. For example, it is possible to feed the same sine wave into both input A and input B, and determine the period of either the positive half-cycle or the negative half-cycle, by setting the trigger-slope selector switch of channel A to one polarity and that of channel B to the other polarity.

This feature also permits the use of the "PERIOD A-B" mode for phase measurements, and extends the range of these measurements beyond 180° by appropriate slope-polarity selection.

The slope-polarity selection feature also permits measurement of the pulse width of isolated single pulses (such as the "dwell time" of a vibrating contact) by triggering channel A on the positive-going rise-time of a pulse, and triggering channel B on the negative-going fall-time of the same pulse.

In general, period measurements are particulary useful in the precise determination of frequencies that are too low for measurement by ordinary techniques.

NOTE: Throughout this discussion we have referred to signal "pulse". It should be understood that the input amplifier circuitry is such that it accepts signals of widely varied characteristics and shapes them into pulses suitable for use in the gate and counting arrays. Thus, the input signal may be sinusoid, a trapezoid, a triangular wave, a square wave, etc.

The range of the period measurement provided by this instrument is extremely wide because the internal generator it contains makes available frequencies from 1 megacycle per second down to 0.1 cycles per second in eight decade steps. Thus, it is possible to measure periods as long as 999,999 x 10 seconds, or almost 10 million seconds! At the upper end of the available frequency range, period increments are measured in microseconds per digit displayed.

Before proceeding to the next functional explanation, it would be well to examine the circuitry of which the wide-range signal generator mentioned above is composed. The block diagram of figure 4-6 is a representation of this signal generator.

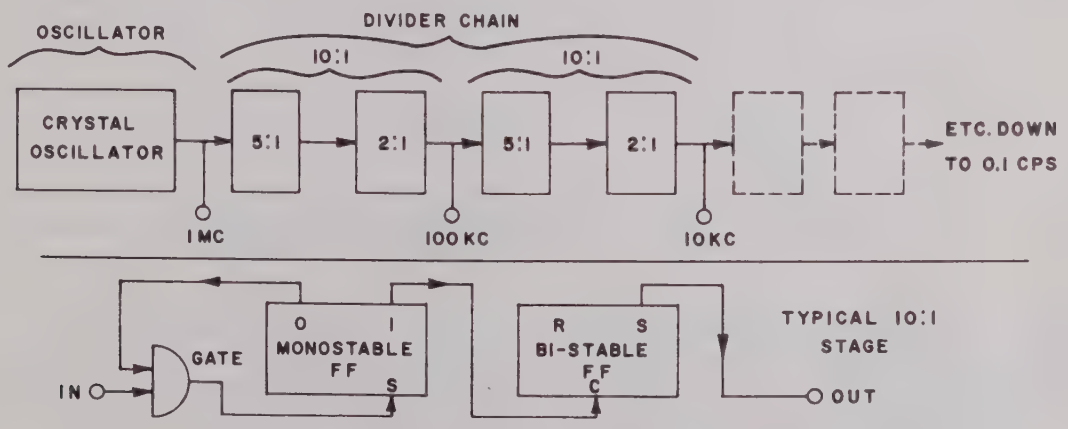


Fig. 4-6 Simplified Block Diagram #4 Internal Signal Generator

A one megacycle crystal is enclosed in an oven to stabilize its frequency over long periods of time. (Provisions are included in this oscillator circuit for calibration against the primary-frequency standard provided by NBS station WWV). The output of this crystal oscillator provides the one-megacycle signal required by many of the measurements performed by this instrument. This one megacycle output is also fed to a "count-down chain"

The count-down chain consists of a series of 10:1 frequency-dividing circuits. Each 10:1 step in the chain is actually split into two divisions: a 5:1 divider feeding a 2:1 divider.

The 2:1 division is performed by feeding pulses into the complementing input of a flip-flop of the type we have described earlier for other applications in the instrument. The 5:1 divider circuit consists of an AND gate and a monostable binary flip-flop.

The monostable flip-flop operates in the following manner: when an input pulse is received on its set input terminal, it changes state. It then retains the new state for a period of time determined by certain of its circuit elements. After the predetermined length of time has elapsed, the circuit recycles, returning to its original state. In the 5:1 divider application, the period of time required for recycling is designed to be approximately 4.5 pulse intervals. That is to say, if the one megacycle signal is to be divided by 5:1, the associated monostable flip-flop circuit would be designed to return to its original state in approximately 4.5 microseconds. Thus, after an input pulse was received, triggering the monostable flip-flop, it would "relax" shortly after the fifth pulse has been produced by the one megacycle source, but shortly before the sixth pulse would have been generated. The output of the reset terminal of the monostable flip-flop is connected back to one of the two inputs of the AND gate. The other input of the AND gate is fed from the frequency source which is to be divided by five. Thus, when the first pulse enters the gate, the gate is open, because the monostable circuit is in its original state. When the first pulse triggers the monostable flip-flop, the gate closes, and does not again open until after it has rejected the second, third, fourth, and fifth pulses. Then the gate opens, (half-way in time between the fifth and sixth pulses) and the sixth pulse is accepted, repeating the entire cycle. Thus, every fifth input pulse is fed to the 2:1 divider, in this way producing an output pulse for every tenth input pulse.

It is important to note that there is little if any chance of inaccurate division, despite the fact that the 5:1 divider element is not digitally controlled. This element is

nominally set to 4.5 input pulse intervals. It would have to drift more than 11% in time period in either direction in order to generate a false division. The extreme derating of the components in this instrument, and the careful design of the monostable circuit, preclude this possibility except in the case of catastrophic failure of one of the circuit elements.

Before leaving the subject of period measurement, it is worthwhile noting that the panel control which selects the particular frequency output desired from the internal generator is calibrated directly in seconds of period between two successive pulses. This calibration renders the reading of an output result extremely easy, and inherently error-free. One simply multiplies the reading on the Nixie display by the period selected on the "time-interval" knob, and the answer is obtained directly in seconds.

If the particular internal generator output selected to gate the counting interval was the 0.1 cps output, the result would be the number of cycles in ten seconds, or would have to be divided, in other words, by 10 to yield cycles per second or pulses per second. On the other hand, if the 10 cps internal generator output had been selected, the Nixie display would have had to be multiplied by 10 to yield cycles per second or pulses per second.

The logic of this latter measurement is now obvious: by interchanging the source of pulses and the gating control, we have constructed a circuit which will measure frequency rather than period. Note that in both cases the internal generator controls the accuracy of the measurement. Since the count-down chain preserves the accuracy of the crystal oscillator for all frequencies generated, the time intervals generated by its gating action are equally accurate, regardless of the particular output frequencies

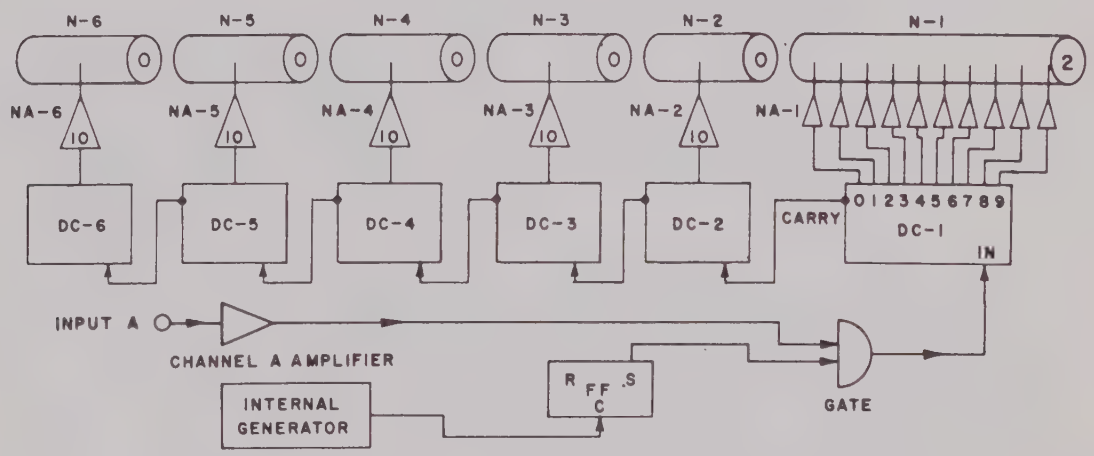


Fig. 4-7. Simplified Block Diagram #5 Frequency Measurement

There is very little difference between the circuitry employed in this instrument for the measurement of frequency and that employed for the measurement of period. This can be seen by comparing the block diagram of figure 4-3, in which period measurement was first described, with Figure 4-7 above. The pulses of waveforms representing the frequency to be measured are fed into the Input A terminal, amplified and shaped by the channel A amplifier, and fed through an AND gate to DC-1, the first decade counter. The other input to the AND gate is provided by the gating flip-flop which in turn is driven by the particular output of the count-down chain selected by the "Time Interval" switch. Thus, the counter records the number of input cycles or pulses that have occured between two successive output pulses of the internal generator. If the internal generator output selected happens to be the 1.0 cps output, the instrument directly reads the number of input cycles fed to input A in a one-second interval, and the output result is direct-reading in cycles per second or pulses per second.

selected to govern the interval of time during which the incoming pulses are counted. Thus, if the internal crystal oscillator is accurate to ±1 part per million, the overall measurement is accurate to ±1 ppm ±1 count, or a total of ±2 ppm for a full count on the Nixies.

FREQUENCY RATIO MEASUREMENTS

If we substitute, in the block diagram of figure 4-7, above, an external source of timing, and feed it through input B and amplifier channel B, we will have constructed a configuration that permits determining the ratio of the frequency on input B to the frequency on input A. In order to follow the functioning of this circuit, let us suppose that the frequency on input B is 500KC, and the frequency on input A is 10 KC. The pulses applied to input B, after shaping and amplification, are fed to one input of the AND gate. The pulses fed to input A operate the gating flip-flop which, in turn, operates the other input of the AND gate, permitting the frequency fed to input B to be counted during the interval between two successive pul-

ses on input A. Thus, after the first of two pulses on input A, the AND gate is opened, and a total of 50 ±1 pulses will be counted by the decade counters before the next pulse is fed to input A, closing the gate. Thus the ratio of input B frequency to input A frequency is directly read out as an integral number on the Nixie display.

This functional mode of the instrument is extremely useful in analysis of complex pulse programs, such as are encountered in computing and digital control devices. For example, input B can be fed from the "clock pulse generator" of a data-processing device, while input A can be fed from any one of a number of sources of lower frequency (longer time interval) that are supposedly synchronized to the clock pulse. The exact relationship between these lower frequencies and the clock pulse frequency is then read directly on the Nixie display.

ACTIONS PER TIME INTERVAL

There is no difference between the block diagram (or the behavior) of the instrument for the measurement of actions per time interval and that for measuring frequency, except that the results are interpreted differently. In measuring actions per time interval, one normally is working with an aperiodic or intermittent series of "events". The Nixie display then gives the total number of such events that have occurred during the time interval selected. This total may be averaged to yield an average frequency, but there is no way of interpreting the results so as to indicate the highest or lowest frequency contained within the random series of events counted.

SELF-TESTING

In the "TEST" mode of an instrument of such complexity and high inherent accuracy as the APTI-METER, it is necessary that a number of different test programs be employed. The test program designed into this instrument is unique in that nearly every component of every circuit is checked by the program, yet the entire operation requires only the simplest of front-panel control manipulations and requires about one minute to complete.

The block diagram of figure 4-8 shows the circuitry involved in the test program.

Basically, all tests involve counting one of the outputs of the internal generator, while gating the counter "ON" and "OFF" with one of the outputs of the internal generator (the same or a different output, depending on the test performed), yielding various Nixie displays.

The particular test performed is determined by the setting of the "Time Interval" selector switch. The combinations are shown below:

SETTING OF "TIME INTERVAL" SWITCH (Counting Period in seconds)	FREQUENCY COUNTED (Automatically, internally connected)	CORRECT NIXIE READING (nominal — subject to the ±1 count accuracy rating of the instrument)
10^{-6}	1MC	000001
10^{-5}	1MC	000010
10^{-4}	1MC	000100
10^{-3}	1MC	001000
10^{-2}	1MC	010000
10^{-1}	1MC	100000
1.0	100KC	100000
10	10KC	100000

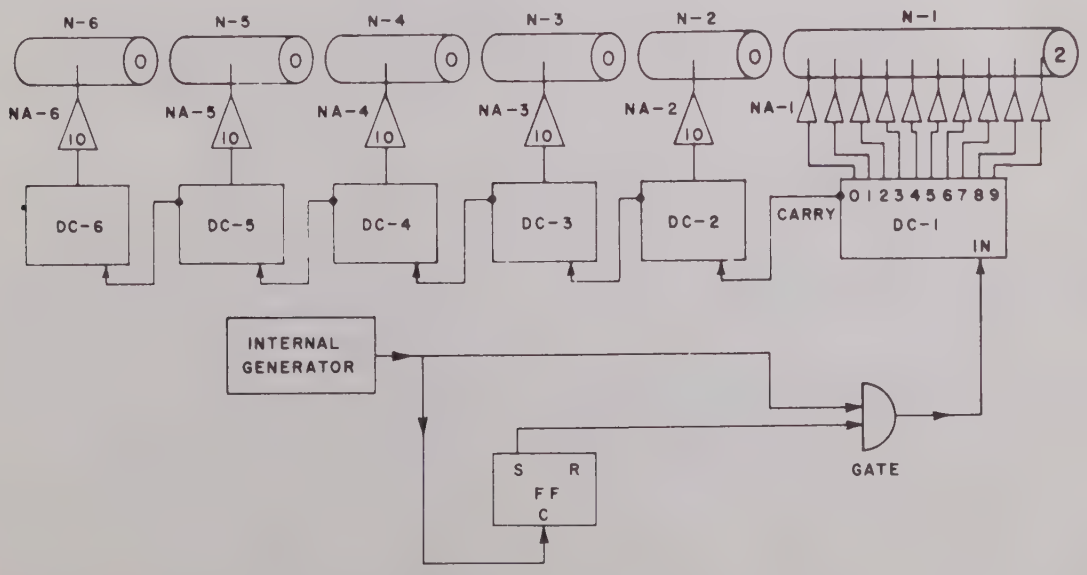


Fig. 4-8. Simplified Block Diagram #6 – Self-Testing

Since the circuitry employed for the test is identical to that employed in the FREQUENCY measuring mode, there is no need to review its behavior here.

MISCELLANEOUS

We have now discussed all of the major operational arrangements which may be "constructed" from the circuitry available in the instrument. It would be well, at this time, to review a few auxiliary circuits that are used to implement the accessory features of the instrument. For example, no mention has been made of the fact that the Nixie readout has a controllable display time. The block diagram of figure 4-9 illustrates the circuitry which provides this feature.

Resetting the first flip-flop acts to reset the delay circuit and also to reset the first gate flip-flop. This action restores the counter to readiness, and permits further counting. The process is free running, in the sense that the counting, display, and delay functions continue indefinitely unless the source of time is removed.

Note that the entire process of display-time delay and resetting is triggered by the resetting of the gate flip-flop, which occurs when the count is complete. Thus, the time required for the instrument to reach a total count is not included in the display delay time. This delay time is constant, regardless of the number of counts loaded into the decade counter.

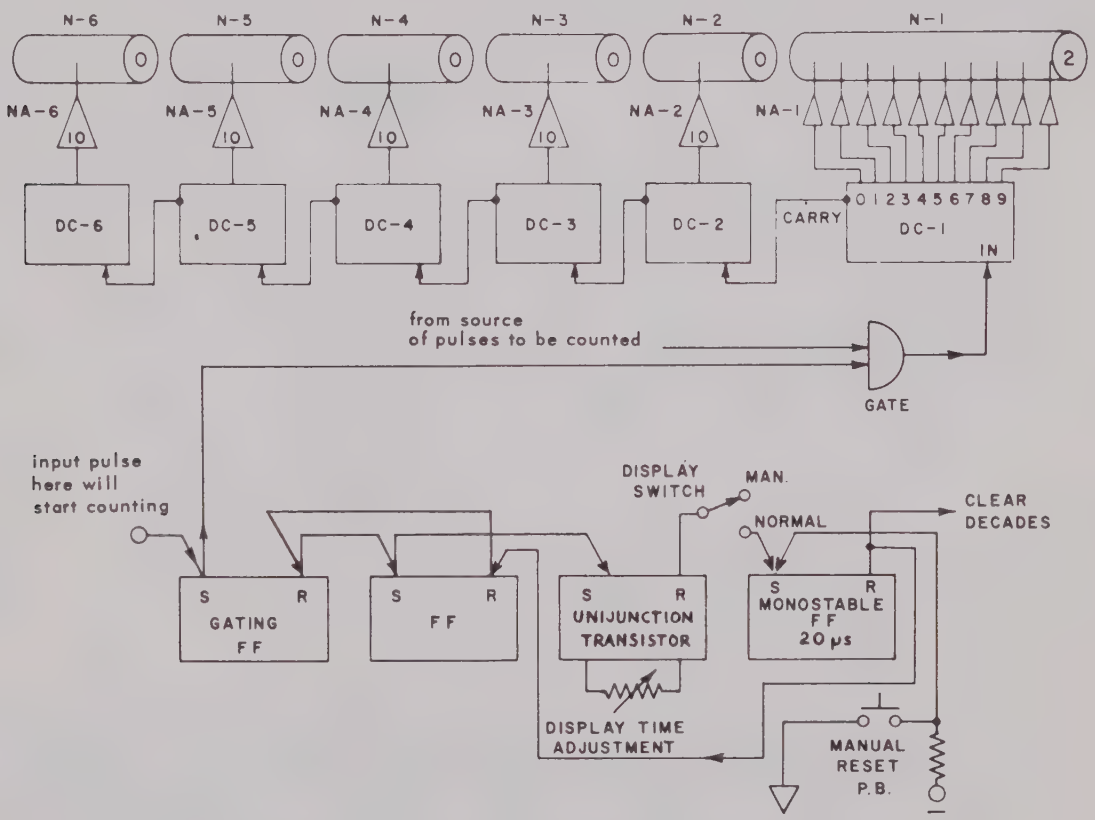


Fig. 4-9 Simplified Block Diagram #7 – Display Time Control

The same flip-flop that turns the counting gate on and off is used, at the end of each counting interval, to set another flip-flop.

This flip-flop, in turn, triggers a unjunction transistor with adjustable "relaxation" time. This transistor starts a time-delay process, which is adjustable by adjusting one of the delay parameters (resistance) in the circuit. At the end of the delay interval, a second flip-flop is set, resetting the first, and also providing an output pulse which acts to reset all of the decade counters. (This latter pulse is fed to the "clear" terminals of each of the decade counters.)

If desired, the display may be held until reset manually. In fact, each successive count reading may be manually triggered. This is accomplished by rotating the display time control to the extreme counter clockwise position, at which point it operates the "Manual Display" Switch. In this mode, the delay circuit is disconnected from the decade-resetting flip-flop, which is, instead, operated from a momentary-contact push button. This push-button is connected to a source normally negative which can be brought positive by operating the push-button. This push-button sets the reset flip-flop, causing the clearing of all decades. At the same time it resets the gate flip-flop, which readies the counter for a new measurement.

Another auxiliary feature provided by the instrument is a buffering amplifier which is fed from the particular time base selected on the time interval switch, and which provides a "Frequency-Standard" output. This output is a sine wave in the one-megacycle position, and essentially a square wave in the 100KC, 10KC, 1KC, 100 cps, 1cps, and 0.1cps positions. This feature permits the secondary standard frequencies generated by the instrument to be used for external purposes. It also permits the use of these frequencies at other than the decade steps indicated, since the square wave outputs are rich in harmonics, and contain useable, ultra-stable signals up to 10 megacycles. Since the buffering amplifier completely isolates this output from the internal circuitry which generates the signal, both the counter function and the frequency-standard function of the instrument may be simultaneously employed, without interaction. In fact, the buffering is so complete that the instrument may be operated with the frequency output continuously shorted, without either damage or interaction.

Finally, a very useful accessory output is provided by feeding into a buffering amplifier the "set" output of the gating flip-flop. The output of this amplifier is available at the rear of the instrument, for external synchronizing and triggering use. This output is positive during the counting period, and negative at all other times.

One interesting application of this pulse is found in period measurement. Using an oscilloscope with either Z-axis modulation, externally-triggered sweep, or a dual-channel (or summing) input configuration, the exact point at which period measurements begin and end may be determined (and adjusted by means of the trigger level slope, and sensitivity adjustment) to a degree of accuracy limited only by the oscilloscope circuitry.

V CIRCUIT THEORY

We have now examined in some detail the functional behavior of the instrument in all of its operating modes. Let us now examine the circuitry employed to implement that behavior.

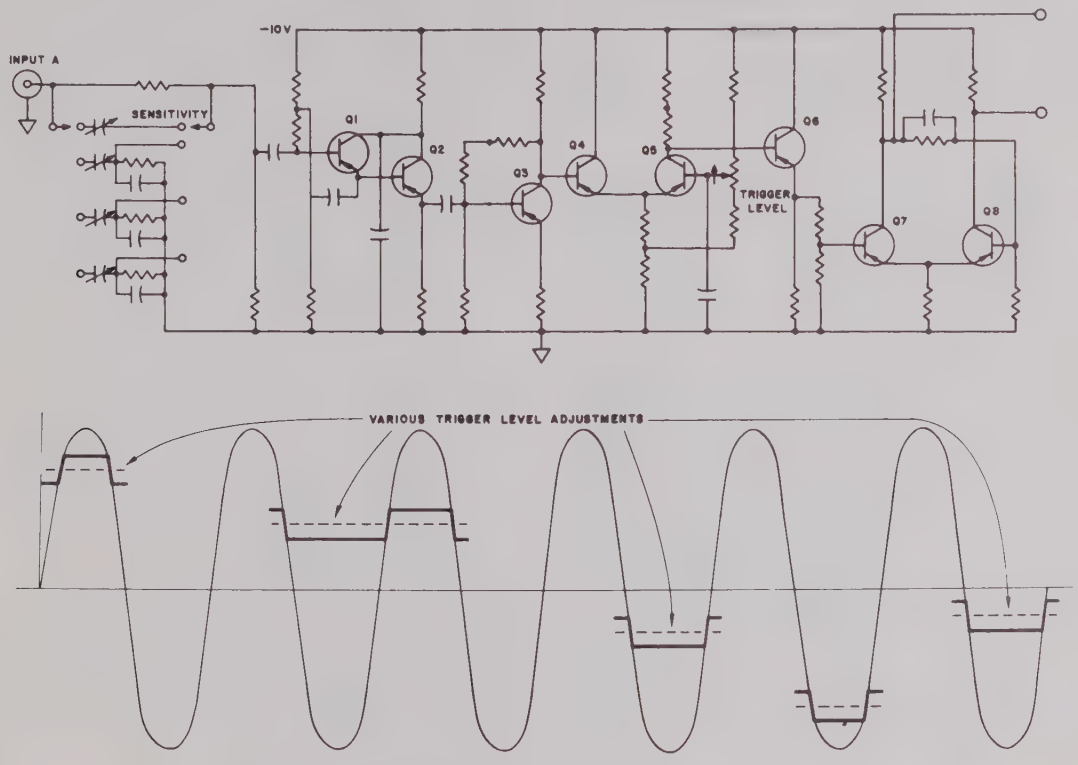


Fig. 5-1 Simplified Schematic Diagram – Signal Amplifier

Figure 5-1 is the schematic of one of the two signal amplifier channels. The input signal is fed to a four-step, frequency-compensated resistive attenuator providing ratios of 1:1, 1:10, 1:100, and 1:1000. Q1, the input transistor, functions as an emitter follower, driving another emitter follower, Q2. The output of Q2 is RC-coupled to the base of Q3, which functions as a high-gain voltage amplifier, the output of which is fed to the special amplifier circuit Q4 and Q5.

This circuit is unusual in that it is a stable, high-gain, voltage-selective amplifier, having the ability to select a particular small portion of the input signal excursion, and to amplify it without being affected by the size of the total input signal fed to Q4. The particular portion of the input signal selected by this amplifier is determined by the setting of the Trigger Level Control potentiometer, which determines the potential of the base of Q5. The base potential of Q5 will always be a fraction of a volt more negative than the emitter potential of Q5, as long as Q5 conducts, and this relationship also determines, therefore, the zero-signal emitter potential of Q4. Thus, any signal which tends to swing the base of Q4 more than a fraction of a volt more positive than the zero-signal common-emitter potential will cut off Q4 completely.

On the other hand, any signal which attempts to swing the base of Q4 more than a fraction of a volt more negative than the zero-signal common-emitter potential will cut off Q5. Assuming a large input signal to Q4 (that is to say, considerably larger than a volt or two) it is thus obvious that, for the amplified output that appears at the collector of Q5, the effective input signal will be that portion of the input signal which immediately surrounds the common-emitter potential that has been set up on the trigger-level potentiometer. The graph drawn on Figure 5-1 illustrates the effect of adjusting the trigger level control to various settings, with a relatively large signal fed to the base of Q4.

Perhaps the most interesting feature of this sampling amplifier is the fact that it accomplishes the variation in sampling point without significantly altering the peak-to-peak output amplitude. The output of the sampling amplifier is direct-coupled to the base of the Schmitt-trigger input transistor Q7.

Q7 and Q8 make up a form of the Schmitt trigger circuit, which may be defined as a monostable binary with input-level hysteresis. A simple way of explaining the behavior of this circuit follows. Without input signal, Q8 is normally conducting and Q7 is normally cut off. If the potential of the base of Q7 is slowly made more negative, a level is ultimately reached at which Q7 begins to conduct. The

reaction of the binary is similar to that of symmetrical flip-flop, in that once it begins to change from its stable state to the opposite state, the change is rapid and has an "avalanche" characteristic——that is, the initial current that begins to flow in Q7 makes the potential of its collector more positive, which tends to reduce the current in the base of Q8, which makes the common-emitter potential more positive, tending to increase the current in Q7 still further, tending to reduce the current in Q8 still further, etc., until Q8 is completely cut off and Q7 is conducting fully.

This condition will continue as long as a negative signal of sufficient magnitude exists at the base of Q7. If the input voltage is now slowly changed back toward the original value (in the positive direction) it will be found that it must be driven beyond the value at which the original triggering occurred. This is true because the common-emitter potential established during the second state is more positive than that which was established originally, since the "full on" current of Q7 is lower than the corresponding current in Q8, due to the difference in their collector resistors and base-coupling circuits. This difference in critical input levels is called "trigger hysteresis," and serves the very important function of distinguishing between the desired triggering signal and smaller "noise" disturbances which may appear on it. In order for such random noise disturbances to effectively trigger the Schmitt circuit, they would have to be larger than the hysteresis of the trigger, which is unlikely, since the circuit has been designed for relatively large hysteresis.

The use of the sampling amplifier to limit the signal excursion fed to the Schmitt trigger has the added effect of eliminating the annoying level shift encountered at high frequencies when large signals are "self-rectified" at the base of the trigger, and the average level of this rectification is stored across circuit capacitances. The ease of adjustment of this instrument at high frequencies is greatly enhanced over that of conventional circuits by this limiting.

The discussion of hysteresis vs noise given above supports the statement in the operating instructions which advises the use of the lowest possible sensitivity that will still effectively trigger, so that the effects of noise components are minimized.

The basic flip-flop circuit of Figure 5-2 is not only the heart of the decade counters employed in this instrument, but it is also used, in slightly modified form, in several other circuits we shall presently describe. The basic circuit has bilateral symmetry; every odd-numbered component corresponds (within normal tolerances) to every even-numbered component, so that the circuit to the left of R9 is essentially identical to that on the right of R9. (R9 is unique). This circuit has two stable states:

1. With Q1 conducting heavily, and the potential of points A and Y more positive than the corresponding potentials of B and X. Q2 is cut off (because point Y is more positive than point Z) and its collector potential is nearly that of the power supply, except for the small potential drop due to the current drawn by R4 and R8 through R2. (This current is small compared to the current drawn through R2 when Q2 conducts heavily.) In this state, the flip-flop is "RESET". (Reset terminal more positive than set terminal.)
2. With Q2 conducting heavily, and Q1 cut off. Points B and X are more positive than points A and Y, respectively, and the potential of A is nearly that of the power supply. The circuit conditions are exactly reversed. In this state, the flip-flop is "SET".

In order to understand the behavior of the circuit, let us assume that the flip-flop is RESET. Under this condition, a positive pulse fed to the "complementing" input would tend to raise the potential of both bases. The base of Q2, however, would not be responsive to this signal, because Q2 is already cut off. Further, the "steering" circuit R8, CR2 has biased the C4, CR4 branch of the circuit against incoming pulses. Diode CR3, however, provides an effective path for an input signal, through C3, and the potential of the base of Q1 is made more positive, lowering the base circuit current of Q1.

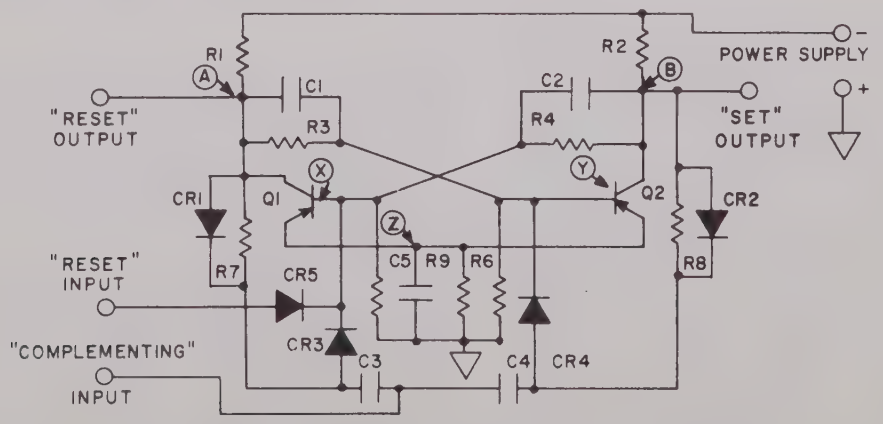


Fig. 5-2 Basic Flip-Flop – Simplified Schematic Diagram

Once the base current of Q1 has begun to drop, a series of events occurs that result in an "avalanche" effect, the result of which is to reverse the state of the flip-flop. Let us follow this avalanche cycle around the circuit. A small decrease in the current in the base of Q1 will result in a correspondingly smaller collector current drawn through R1. This makes the potential of point A, (and, consequently, the potential of point Y) less positive. Lowering the potential of point Y will tend to start the flow of current in the base of Q2, raising the potential of point B and, consequently, the potential of point X. Raising the potential of point X tends to further reduce the base current of Q1, further reducing the potential of points A and Y, and so on through the same cycle. The ultimate result of this self-perpetuating avalanche effect is to switch the flip-flop from the "RESET" state to the "SET" state. Q2 now conducts heavily, and Q1 now is cut off. The entire avalanche action described above is normally accomplished in a very small fraction of a microsecond in flip-flops designed for high-speed counter applications. The process of switching is assisted by the presence of C1 and C2, which effectively bypass R3 and R4, and make available the charge stored on them (the voltage drop across these resistors) to absorb minority carriers which have accumulated around the base-emitter region of the saturated transistor, and also reduce the effect of the input capacitance of the transistors on the switching time.

When the flip-flop has been set, a subsequent signal on the complementing input will operate through CR4, C4, and the base of Q2 in exactly the same manner as they did through CR3, C3, and the base of Q1. This symmetry guarantees equivalent performance on successive input pulses, and makes possible complementing of the flip-flop under high-speed conditions.

The current through R9 is essentially constant (since only one transistor of a pair is conducting at any one time, except for the transition interval) and the potential at point Z is essentially constant. The only variations in the potential of point Z occur when unsymmetrical conditions exist in the circuit, or when unsymmetrical behavior occurs during the transition, or switching state. These conditions cannot disturb the stability of the circuit during low-speed switching service, but they can be disturbing in the very highest frequency applications. For this reason, a small capacitor, C5, bypasses resistor R9, thus guaranteeing the stability of its voltage during the transition state.

Note that an additional input (the "Reset" input) has been provided. When a positive pulse is fed to this input, it forces the flip-flop to the "RESET" state, through CR5.

Let us turn our attention next to the circuitry implementing the element we have called the decade counter. We shall begin by an examination of Figure 5-3, which is a logic diagram describing the interconnections of elements which go to make up a decade counter.

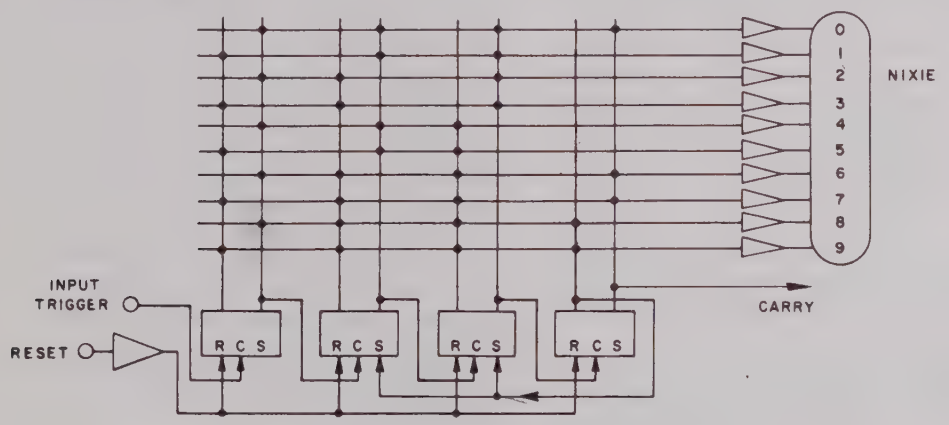


Fig. 5-3 Logic Diagram – Decade Counter.

It will be seen that there are four symmetrical flip-flops (of the type described earlier) involved in the construction of a decade counter. The outputs and complementing inputs of these flip-flops are so inter-connected as to produce a set of coded voltages on a set of 10 output lines. The code is very simple — the voltage on the line which represents the particular count stored in the decade (e.g. line number 3 after three input pulses have been stored) is positive, while all the rest are negative.

The flip-flops are so interconnected that their cycle repeats after 10 pulses have been fed to the input of the counter circuit. This is accomplished by a feedback interconnection which circumvents the normal behavior of a four-stage scale-of-two counter; for such a counter, would, of course, have a total count capacity of 16 counts rather than 10.

Remembering that these are symmetrical flip-flops of the type just described, let us trace the behavior of the counter circuit. To begin with, a previous pulse on the "RESET" line of all four flip-flops in parallel has reset them all. Thus, all SET output terminals are negative, and all RESET output terminals are positive.

The first input pulse sets the first flip-flop; the second input pulse resets it, and sets the second flip-flop; the third input pulse sets the first flip-flop again, leaving the second one set. The fourth input pulse resets the first flip-flop, resetting the second, which sets the third.

To summarize at this point, we see that after the arrival of the fourth count the flip-flops are in the following condition: #1 is reset, #2 is reset, #3 is set, and #4 is reset.

To continue, we see that the fifth input pulse sets the first flip-flop, leaving the rest unchanged. The sixth input pulse resets the first flip-flop, setting the second. The seventh input pulse sets the first flip-flop. Now all of the first three flip-flops are set, and only the last is reset.

Normally, at this point, the next pulse would result in the expected behavior: that is, the fourth flip-flop would be set, and all the other three would be reset. However, a feedback connection has been provided so that the act of setting the fourth flip-flop also sets the second and third. This action actually controverts the normal order of things, and has the affect of adding six extra counts to the normal 16-count action of a four-stage binary counter, reducing its actual count capacity to 10 counts.

The eighth pulse, therefore, leaves the first flip-flop reset and all the rest set. The ninth and last pulse in the sequence sets the first flip-flop, so that all flip-flops are now set.

The next pulse to enter the counter (the tenth pulse) resets all four flip-flops, so that the counter has been returned to its original state. When this occurs, we require (it will be recalled) a "carry" pulse to be fed to the next decade. This pulse is provided by the fourth flip-flop as it resets. Its Reset terminal goes positive at that instant, and a positive pulse is delivered to the Trigger Input terminal of the succeeding decade counter.

0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	1	1	1
9	1	1	1	1

Fig. 5-4 Decade Count Sequence

The count sequence described above is illustrated in the chart of Figure 5-4. Observe that each count results in a unique pattern of output voltages on the flip-flops. These patterns are created by designating a reset flip-flop as one which is in the "0" state, and a set flip-flop as one which is in the "1" state.

Next, let us consider how the circuit "decodes" the various states of the four flip-flops in such a manner as to develop a positive voltage on one (and only one) of the ten output lines when the count stored in the decade is such that the particular output line should have a positive voltage on it. Referring back to the logic diagram of Figure 5-3, we see that a matrix has been established in which the vertical lines are the eight outputs of the four flip-flops. The horizontal lines are the ten output lines.

The lines are shown interconnected by heavy dots drawn at certain points. (Where the dots are not shown, the matrix is not connected.) If we assure that a horizontal line is energized when (and only when) all of the dots connecting it to flip-flops are in the "1" state, we will see that the requirements for decimal readout of the counter are satisfied. For example, the zero line is energized only when all four flip-flops are reset, a condition that is satisfied only when the counter has been cleared to zero.

Again, the #6 output line is permitted a positive voltage only when flip-flops 1 and 4 are reset, and, simultaneously, flip-flops 2 and 3 are set. An examination of the chart of Figure 5-4 shows that this is, indeed, the sixth-count output state.

Thus the "decoding matrix" satisfies the requirements for decimal readout of the modified binary counter constructed from the four flip-flops used. We can now turn our attention to the actual circuitry employed to implement the functions described in the block diagram we have been discussing.

In the schematic on page 7-16 (see Section VII "Servicing") the four flip-flops are drawn along the bottom of the diagram. They are preceded by a single-stage inverting amplifier, consisting of C1, R1, Q1, R2, R3, and C2. This amplifier produces a powerful, sharp reset pulse which "clears" all four flip-flops by driving them to the reset state whenever a negative pulse is applied to the input of the amplifier.

The input signal fed to the decade counter is applied to the complementing input of the first flip-flop. This flip-flop is identical to the one discussed earlier in this section, and we need pay no further attention to it, except to note that it consists of the circuits involving Q2 and Q3. The reset output of this flip-flop (the collector of Q3) is fed to the complementing input of the second flip-flop (Q4 and Q5) and the reset output of the second flip-flop is connected to the complementing input of the third, and so through the sequence. The feedback path from the fourth flip-flop set terminal is fed to the second and third flip-flops through CR24 and CR15, respectively. As noted earlier, this feedback is not directly obtained from the fourth flip-flop but appears as a pulse which is developed as the fourth flip-flop (slightly delayed) transfers from RESET to SET. This permits the flip-flops which are to receive the feedback signal to first reset and immediately be set again.

The remaining circuits in the four flip-flop stages are identical in every way to those described earlier except for the anomaly just noted in flip-flop 4. This additional circuit, which consists of C23, R43, and R32, insures that the feedback signal will not conflict, in time or energy-level, with the "normal forward" counting pulses.

The decoding matrix employed in this decade counter consists of resistors R48 through R82 inclusive. These form a group of so-called "NAND" circuits, connected to the bases of Q10 through Q19 inclusive. Q10 through Q19 are the Nixie amplifiers. They perform the function of raising the potential of the particular Nixie electrode which is to glow during the corresponding counter state.

The emitter potential of all the Nixie amplifiers is established by voltage divider R46 and R47. The base potential required to cause an output appears when all the resistors tied to that base are connected to terminals that are positive with respect to the emitter potential. When this is true, that transistor conducts, causing the corresponding Nixie electrode to glow. All other transistors, it will be found, by examination of the matrix, have their bases connected to at least one resistor which is terminated in a negative voltage. Thus, the decoding process is implemented by correct connection of the lower terminals of the resistors comprising each "NAND" gate.

The "carry" output appears on Trigger Output terminal 4 when the fourth flip-flop resets, representing the transition from "9" to "zero".

Figure 5-6 shows the schematic diagram of the 1-megacycle oscillator which is the heart of the internal generator in this instrument. Q8 is connected in a crystal oscillator circuit of a modified Clapp type. The resonant frequency of the crystal circuit may be slightly modified by the adjustment of C7. This adjustment is provided so that the crystal may be set exactly on frequency, when the instrument is calibrated against a primary standard, such WWV.

The output of the crystal oscillator is fed to an emitter follower, Q7, the output of which is capacitively coupled through C10 to a grounded-emitter voltage amplifier stage, Q6, which drives emitter-follower Q5, the output of which is developed across R19. Note that this circuit is extremely well buffered against any loading effects, and has sufficient voltage gain so that the oscillator may operate at a relatively low output level, which enhances its stability.

The overall stability of this circuit is extremely high, due to the fact that the crystal, which chiefly determines the operating frequency, is contained within a temperature-regulated oven of advanced design. The crystal is of a low-drift type, with exceptionally high initial accuracy. The circuit is such that the effects of changes in transistor characteristics are very much degenerated primarily by de-coupling, so that the performance of the oscillator will not exhibit any significant degradation over a wide range of ambient temperatures, component values, and power supply variation.

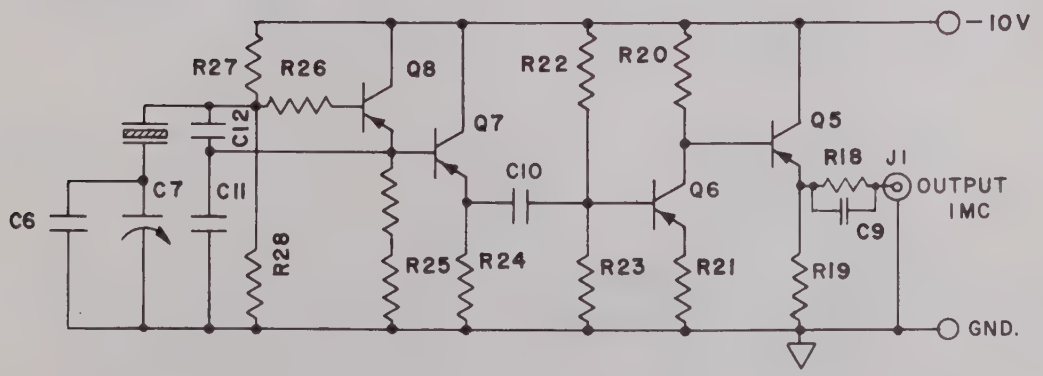


Fig. 5-6. Simplified Schematic Diagram – 1MC Oscillator

Figure 5-7 shows one stage of the circuitry used throughout the count-down of the internal generator. The circuit involving Q3 and Q4 is that of the 5:1 divider, while the circuit to the right, consisting of T5 and T6, is that of the 2:1 divider.

The 5:1 divider is actually a monostable form of the symmetrical flip-flop discussed earlier in this section. R17 is the common-emitter resistor, as in the symmetrical circuit. R13, C7, R14, R10, R12, C9, D4, R15, and R16, all perform the same function as described earlier for the symmetrical flip-flop.

The principal difference between the circuits is seen by examining the circuitry which couples the collector Q3 to the base of Q4. Instead of a direct connection, this circuitry contains an R-C delay network consisting of R11, R12, and C6. Diode CR5 completes the coupling path. This circuit has only one stable state: that is, with Q4 conducting heavily, and Q3 cut off. When a positive pulse is received on the input line, and coupled by C9 and CR4 to the base of Q4, it cuts Q4 off, and the avalanche behavior described previously for the symmetrical flip-flop occurs, setting the flip-flop, and temporarily cutting off Q4. Q4 remains off until capacitor C6, which was previously uncharged, charges to the voltage drop across R10, through R12, and R11. When the potential at the base of Q4 has become sufficiently negative so that Q4 can begin to conduct, the circuit "relaxes" to its original stable state, in which Q3 is cut off. The time required for this relaxing to occur depends primarily upon the values of C6, R12, and R11, since R10 is relatively low in resistance. Note that until the stable state is reestablished, pulses arriving on the input line are ineffective. When the stable state has been reestablished, the next pulse arriving on the input line begins the cycle all over again. In the design of a 5:1 divider, we proportion the time constant C6 (R12 and R11) so that it requires approximately 4.5 pulse intervals for the circuit to resume its original state. This permits, as explained in thd previous section, 5:1 division with high accuracy and dependability. R11 is the adjustment that permits setting this circuit to 4.5 pulse intervals. (See ROUTINE MAINTENANCE section for details.)

Each time Q3 conducts, a positive pulse is applied to the complementing input of the symmetrical flip-flop. The output terminal of this stage, and hence of the 10:1 divider, is the collector of Q6.

Figure 5-8 shows the power supply employed in this instrument. Three output voltages are developed: A high-voltage, low-current supply for the Nixie indicators, a low-voltage, high-current supply for switching circuits, and a slightly-lower voltage supply, derived and decoupled from the main low-voltage supply, and having lower ripple, for powering the input stages of the amplifiers.

Input power is applied to the primary of T1 through the fuse F1 and the power switch S2. The secondary winding 9-10 feeds a silicon rectifier, CR8. The output of this bridge rectifier is filtered and fed directly to the Nixie circuits without regulation, through current-limiting resistor R9. Winding 8-9 silicon rectifier CR8, and zener diode CR6 with its loading resistor R8, furnish regulated 25VDC. (These components, and blocking diode CR12, are included in the Apti-meter only when the Printer Readout option is included.)

The low-voltage secondary winding 5-7 feeds a silicon bridge rectifier, CR1-4, which operates into a capacitive filter, C1. The "raw DC" developed across this capacitor is unregulated for either line or load changes, and contains a substantial ripple component. The circuit immediately to the right of capacitor C1 is a simple series-regulator driven by a one-stage error-amplifier. QR is the series-regulator transistor, the voltage drop across which is varied in such a manner as to automatically regulate the voltage between its emitter and ground. The regulating action is accomplished by varying the base current in QR in an appropriate manner.

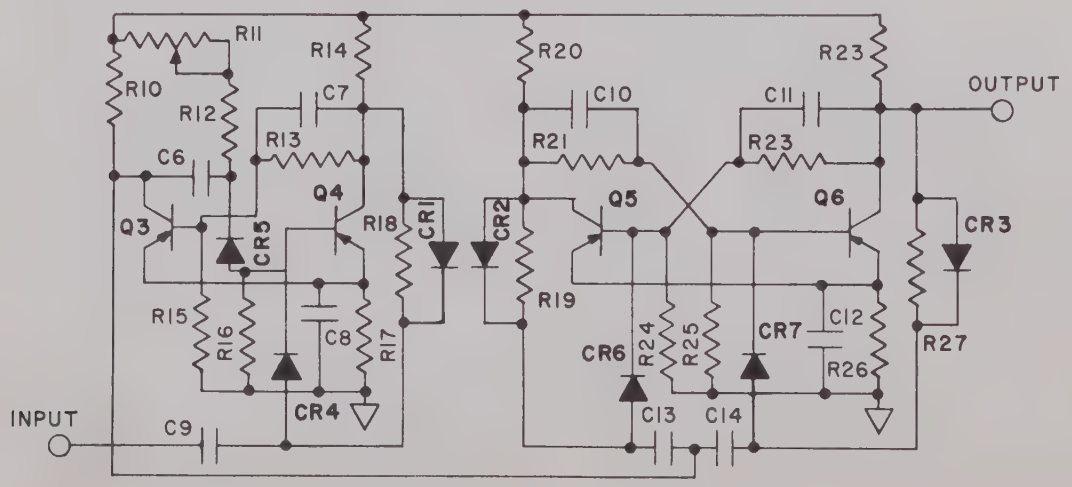


Fig. 5-7- Simplified Schematic Diagram – Count-down Chain

The base current of QR is the collector current of Q1. Q1 is the voltage amplifier. The input signal to Q1 is the difference between a reference voltage and a sample of the output voltage to be regulated. The reference voltage is derived from the voltage drop across a zener diode, CR5.

The zener diode is operated from the regulated power supply through resistor R2. (A zener diode is a semiconductor diode which develops a relatively constant potential in the inverse direction over a wide range of inverse currents). In this circuit, CR5 is exposed to only a very small variation of current, since the principal source of current through it, R2, is operated from a fixed voltage supply. The small variations in the current in CR5 caused by the varying emitter current of Q1 are negligible compared to the current through R2 and a very stable source of reference voltage is established across CR5. The base of Q1, on the other hand, is driven by the network composed of R3, R4, and R5. This network is so chosen that the voltage developed across the base-to-emitter path of Q1 is just sufficient, at the correct regulated output voltage, to draw sufficient collector current through Q1, so that the base current of QR is just sufficient to furnish the desired output current.

correct operation. The degenerative action of this voltage regulator does, of course, partially filter the raw DC developed across C1.

In addition, the impedance of capacitor C2 is very low at the ripple frequency, and this further reduces the ripple of the -10-volt supply. C2 also performs the function of storing sufficient charge so that peak transient demands in the current drawn from the -10-volt supply do not exhaust the ability of the regulator to furnish a regulated voltage. (The response time of the regulator loop is of the order of 50 microseconds. Since the peak currents drawn from the power supply are of fairly short duration, C2 has more than enough capacitance to "smooth out" these demands into a relatively steady average current. The principal function of the regulator, therefore, is to compensate for relatively slow changes in either the line voltage supplying the raw DC, or in the average load current drawn by the circuitry of the instrument.

The circuit to the right of C2 furnishes a low-impedance, low-ripple output for the sensitive input stages of the two signal amplifiers in the instrument. Capacitor C4 establishes a low transient impedance level for this output, and transistor Q2, in combination with capacitor C3 and resistors R7 and R6 combine to form a "de-rippling" cir-

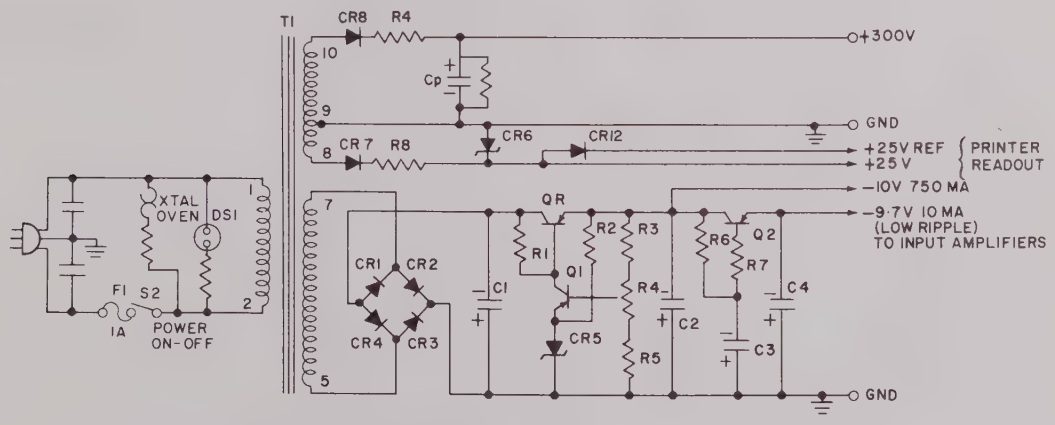


Fig. 5-8. Simplified Schematic Diagram – Power Supply.

When, for any reason, the voltage at the emitter of QR tends to rise, a compensating decrease in the base-to-emitter current of Q1 occurs, reducing the base current through QR, and hence increasing the voltage drop across QR. This sequence of events tends to compensate for the tendency in the voltage at the emitter QR to rise. Although the loop gain around this regulator circuit is relatively low, the circuits in this instrument are relatively insensitive to small variations in power supply potential, and the performance of the regulator is more than adequate to maintain a satisfactorily stable power supply for their

cuit having the same effect as a large inductor. (A sudden rise in the potential of the emitter of Q2 would result in a current rise in that transistor, which would tend to decrease the voltage at the emitter. This is so because the base of the transistor is held at a relatively fixed potential by C3 for short-time changes in the base current of Q2. Similarly, a degenerative action would occur to oppose a drop in the potential of the emitter.) The low impedance characteristic of this circuit, which extends down to very low frequencies, helps to prevent regeneration and interaction in the sensitive amplifiers.

VI ROUTINE MAINTENANCE

The extremely conservative ratings of all components and the careful workmanship employed in the construc- of this instrument render most maintenance procedures unnecessary. A few operational tests and adjustments are recommended, at intervals of 6 months to a year.

SELF-CHECKING

After prolonged storage, or before critical tests are to be performed, a quick run-through of the self-checking ("TEST") procedure at all 8 points is recommended. This procedure is described in the OPERATING INSTRUCTIONS section.

FREQUENCY STANDARD CALIBRATION.

The basic output of the frequency standard is derived from a crystal controlled 1 mc oscillator. The resonant frequency of this oscillator is adjustable over a limited range by varying C7, a crystal trimming capacitor. This capacitor is located beneath the power supply chassis, and is adjusted using a tuning wand (preferably) or a thinbladed, insulated screw-driver inserted through the access port indicated in Figure 7-2. Oscillator frequency is increased by turning C7 counter-clockwise. See addendum for rack mount trimmer location.

The simplest method of calibration of the frequency standare is to "beat" the fifth harmonic (5 mc) of the oscillator against station WWV of the National Bureau of Standards, broadcasting on 5 megacycles. To do so, the 1 mc output of the frequency standard is fed to a receiver turned to WWV at 5 mc and C7 is adjusted until a zero beat note is heard in the speaker or headsets.

A second method is to use WWV as follows: With the Apti-Meter operating, set the TIME INTERVAL selector switch to "1". Connect the frequency standard output to an oscilloscope with a triggered sweep so that the sweep is triggered by the one-second output. Observe the one-second pulse of station WWV by feeding it from a suitable receiver to the oscilloscope. Adjust capacitor C7 for minimum drift of the scope pattern.

Z-axis blanking may also be used as an alternative to observing the WWV pulse itself. The WWV pulse may be used to blank the sweep, which is synchronized to the frequency standard output.

Another method is to obtain a zero-beat Lissajous pattern, using the frequency standard output against that of a secondary frequency standard in the conventional way.

NOTE

Allow the Apti-Meter to warm up at least one hour in a stable ambient temperature environment before making final calibration.

DIVIDER TRIMMING

The 5:1 frequency dividers will probably never drift enough in a year to "slip" to 4:1 or 6:1, but it is good practice to set them to their "safest" adjustment: midway between 4 and 5 pulse intervals. The adjustment of these circuits is accomplished as follows:

1. Set the instrument to TEST, and a time interval of 10^{-5} seconds. The display should read 10 ±1 count.
2. Adjust the 4.5 μsec. trimming potentiometer CW until the display begins to "slip". (This corresponds to a 4:1 division).
3. Noting how many CCW turns of the trimming potentiometer are required, adjust the display until it begins to "slip". (This corresponds to a 6:1 division).
4. "Back off" from the previous adjustment by exactly half of the rotation required to complete step 3. Somewhere along the way, the display will slip back to 10, and one may be confident that the half-way point is very nearly 4.5 pulse intervals.

The process is repeated for each divider, starting with higher frequency one and proceeding in order. The 1 second and 10 second intervals must be used to adjust the two lowest-frequency dividers, of course, but the procedure is the same. The location of the trimming potentiometer is shown in the photographs of the "B" board and "C" board in Figure 7-1. Adjustments to these potentiometers requires a very thin bladed screwdriver. Time interval is shortened by turning the potentiometer clockwise; and lengthened by counter-clockwise rotation.

ADDENDA

Models 361, 361-R, 371 371-R

Section VII Servicing

Page Change

7-1 List of board Numbers and color codes on page 7-1 that are changed are listed below.

TESTS AND ADJUSTMENTS

Board Number	Color Code	Title	Board Assembly No.	Schematic No.
1	Blue	Input Amplifier	A-1004	609-D-103
2	Yellow	Gating Logic	A-1006	609-D-191
3	White	Signal Divider	A-1007	609-D-195
4	Red	100 KHz Decade Readout #22	A-1002	609-D-107
5	Red	100 KHz " " "	"	"
6	Red	100 KHz " " "	"	"
7	Red	100 KHz " " "	"	"
8	Red	100 KHz " " "	"	"
9	Orange	Decade Readout #21	A-1003	609-D-106
10	Violet	Time Base Generator	A-1005	609-D-104

NOTE

Boards not shown in figure 7-1 are:

11	Blue	1 MHz Oscillator	A-1009	609-C-215
12	Black	Power Supply	A-1008	620-C-132

7-2 Power Supply Measurements

At Pin 8, -9.7 V. D. C. and Pin 7, + 300.	Pin 8, -7.8 V. D. C. Pin 7, + 260 V. D. C.
Reset Check, step 3, ---8 seconds	6 seconds
Input Attenuation Tests	
Step 6 -- 0.01V peak to peak	--0.1V Peak to Peak
Step 7 -- the same amplitude	--the same waveform 0.045V Peak to Peak (+20%)
Step 10 -- 0.1 volt square wave	0.045V square wave
Step 13 -- 0.1 volt square wave	0.045V square wave
Step 16 observe a 30 Mv---	Observe a 15 Mv---
Straight Count Functional Check	
Step 3	--Control to "+"
Step 4	Delete--- to "+"

Chart following Step 8 should be deleted and should read:

Input	Timer Internal Setting	Display
External Std.	1.0	1, 000, 000 ±1 *
1Mc Sine Wave	.1	100, 000 ±1
	.01	10, 000 ±1
	10^{-3}	1, 000 ±1
	10^{-4}	100 ±1
	10^{-5}	10 ±1
	10^{-6}	1 ±1

Delete Step 9 entirely

* NOTE: Reading will appear as 000, 000 or 999, 999

Page		
7-3 (cont.)	Nixie Check	
	Step 2-Change "1" to	"Manual"
	Step 3-Change "1" to	"+"
	Step 5-Change "÷100" to	"÷1"
	Following Step 8, after INPUT FREQ add	0.1V. P-P
	Functional Check	
	Step 5-Change "÷100" to	"÷1"
	Following Step 8, after INPUT FREQ add	0.1V. P-P
	First line of chart: change 1, 000, 000 to	1
	Delete Last Line of chart	
	Period A to B Trigger Adjustments	
	1st para. 3rd line: change 'FREQ A' to	'PER A'
	1st para. last line: change 'FREQ ' to	'PER A'
	Step 3-Change "÷100" to	"÷1"
	Step 10-Delete entirely	
	Step 11-Delete words: "square wave"	
7-4	Step 14-delete entirely	
	Period Ax10 Function Check	
	Step 4-Change "÷100" to	"÷1"
	Step 8-should read:	Apply 1Mc, 100 Mv P-P to Channel A input
	Location of Faulty Board	
	In chart: At Pin #10	-7.8 V.D.C.
7-6	Input Channel Attenuator Adj.	
	Step 4, 5, 7 and 8 change Q11	Q13
	Step 9-Change Q3 to	Q5
	Time Base Trimpot Adjustments	
	7th Line: low should be	High
	8th Line: high should be	Low

VII SERVICING

GENERAL

This section discusses servicing and trouble-shooting procedures for the APTI-METER. While the instrument is conservatively designed, and is mechanically rugged and simple, component failures may occur in time. It is obviously impossible to anticipate every conceivable malfunction of a complex instrument, and therefore this discussion will establish a method of trouble-shooting and repair. Before any repairs are attempted it is essential that the user be thoroughly familiar with Sections discussing the circuitry from a theoretical point of view, particularly Sections III, IV, V and VI.

These procedures are designed to isolate trouble to a printed-wiring board or chassis-mounted component. Malfunctioning boards should be returned to the factory for repair and a spare board substituted. If spare boards are not available, contact your nearest TSI representative and he will arrange shipment of a spare from the factory via air mail, or will supply one from his inventory. Be certain to specify the APTI-METER serial number. The diagrams of the printed boards included here are to provide for emergency repairs only.

PRELIMINARY STEPS

It has been well established that a high percentage of the "troubles" encountered in complex electronic equipment are due to, or result from, improper operation. Be certain, therefore, that the following conditions are satisfied before proceeding to the location of trouble:

1) Input power connections are properly made.
2) The POWER ON lamp is not burned out.
3) Input signal connections are properly made.
4) Fuse F1 (back panel) is not blown.
5) The power switch is in the ON position.
6) The APTI-METER has had proper warm-up (see section III)
7) Front panel control settings are proper for the measurement to be made (see Section III)

FRONT PANEL TROUBLE SHOOTING

Most troubles can be isolated by front panel indications, measurements, and observation. The following discussion of symptoms is representative of this trouble-shooting method. It is not complete but it is the result of experience to date. It will furnish a guide; familiarity with theoretical operation of the instrument will permit extension of the method shown.

1) Improper Nixie display in TEST position. In this positon of the Function Selector control each Nixie should display sequentially each digit. If any one Nixie does not, replace the counter board associated with that particular tube. Check Trimpot adjustment in Section VI.
2) All Nixie behave erractically or do not light. Check FREQ. STD. output at front panel BNC as the TIME INTERVAL control is varied. If no output is available check the oscillator and the time base generator boards.
3) Nixies do not reset. Replace board no. 2.
4) Improper Display Time operation. Replace board no. 2.
5) Apti-Meter functions properly in TEST position but does not operate properly in other positions. Check and if necessary replace board no. 1.
6) Nixies "run wild". Check power supply outputs.
7) Two or more numbers of a Nixie light simultaneously. Replace board (4, 5, 6, 7, 8) associated with that nixie.
8) Unit fails to count properly in PER A X 10 but is satisfactory in all other modes. Replace board no. 3.
9) Nixies fail to light. Check power supply.
10) On Nixies and succeeding nixies fail to show proper count. Replace counter board just preceding inoperative Nixie, or board associated with the Nixie.

Intelligent use of the TEST position combined with understanding of the circuitry will greatly facilitate trouble shooting. The following tests are included to permit complete check-out of the Apti-Meter after repair and/or replacement of boards or components.

TESTS AND ADJUSTMENTS

Printed-Wiring

Figure 7-1 (see page 7-7) is a view of the APTI-METER from above with cover removed. Note that all boards are color coded. The following table identifies each board shown in the illustration:

Board No.	Color Code	Functional Circuits
1	Blue	1 cps & 0.1 cps countdown & Input Amplifiers
2	Yellow	Gate and Display Logic
3	White	A X 10 and buffers
4	Black	Counter – 100KC
5	Black	Counter – 100KC
6	Black	Counter – 100KC
7	Black	Counter – 100KC
8	Red	Fast Counter – 100KC
9	Orange	Counter – 1MC
10	Purple	Count Down Chains

With the bottom access plate removed, all pin numbers shown on the schematics and the wiring diagram are available for measurements. A photograph of each board is included for component location (only to facilitate emergency repairs, as noted previously). This section will discuss

trouble isolation using the input-output method. That is, we will examine each board in turn, comparing the measured input and output with that given here, until a reading markedly different from those given is obtained. In this eventuality, the suspect board should be replaced with a spare (known to be good) and measurements remade.

NOTE

The readings given have been obtained under laboratory conditions. Slight variations are likely to exist between them and those of instruments in the field. Do not, therefore, assume trouble-isolation to be complete when readings only slightly different from those given are obtained.

Power Supply

With power applied to APTI-METER, the pilot lamp should light and all Nixies should show an illuminated numeral (or zero). If not, measure the following resistance on the load side of TB1, with input leads disconnected, and with APTI-METER disconnected and power switch OFF;

Pin	Resistance to Ground
2	20 ohms
8	500 ohms
7	100K ohms

Resistances given are minimum; if lower readings are obtained, a short is likely.

Apply power to APTI-METER and measure the following:

Pin	Voltage	
2	-10V ±0.2VDC	(See Figure 7-2 for adjustment)
8	-9.7VDC (nominal)	
7	+300VDC (nominal)	

Functional Boards – Self Testing

General

These functional checks and tests are not intended for routine use; those described in Section III are normal for that purpose. These checks and tests are to be made when improper operation of the APTI-METER is suspected or obvious and board replacement has been made. As a result of the various checks, tests, and adjustments, trouble can be isolated functionally and the board or component at fault replaced or repaired.

Before proceeding with measurements using the APTI-METER and/or prior to trouble isolation, test the instrument using the TEST position of the FUNCTION Selector Control. Proceed as follows:

1. Apply power to APTI-METER (power switch ON)
2. Allow 10-minute warmup.
3. Adjust controls as follows:
   a. Function Selector to TEST position
   b. Time Interval control to 10^{-6} position
   c. Display Time control – centered

Other controls do not affect these tests. Now the Nixie tube furthest to the right should read 9, 1, or 2. All other Nixies should read zero. Then:

4. Set Time Interval control and read display as follows:

Set Time Interval To	Display Should Read
10^{-5}	10 (approx.)
10^{-4}	100 "
10^{-3}	1000 "
0.01	10,000 "
0.1	100,000 "
1	100,000 "
10	100,000 "

Reset Check

With other controls unchanged from previous settings:

1. Set Time Interval switch to "1".
2. Set Display Time control to MIN.
   Nixie display should reset to zero within 0.2 seconds (max) after count ends. Then:
3. Set Display Time control to MAX.
   Nixies should hold display for 8 seconds (min) after count ends. Then:
4. Set Display Time control to MANUAL.
5. Permit APTI-METER to complete count. Nixies should hold display.
6. Depress Manual Reset push button.
   Nixies should clear, displaying zeros on each tube.
7. Repeat steps 4-6 and recheck.
   Nixies should clear ONLY if Manual Reset push button is depressed.

Input Attenuation Tests

To check operation of the attenuators controlled by the Sensitivity Switch, proceed as follows:

1. Turn APTI-METER ON.
2. Set Function Selector to FREQ. A.
3. Set Trigger Slope to "+".
4. Set Trigger Level to mid-range.
5. Set Sensitivity Switch to ÷ 1.
6. Apply a 1 KC square wave, 0.01V peak-to-peak, from an external pulse generator to the Channel A, BNC connector.
7. Observe at pin 12 of Board #1, the same amplitude (±20%) waveform.
8. Set Sensitivity Switch to ÷ 10.
9. Apply a 1 volt, peak-to-peak, square wave from the pulse generator.
10. Observe a 0.1 volt square wave at pin 12 of Board #1.
11. Set Sensitivity to ÷ 100.
12. Apply a 10 volt, peak-to-peak square wave from the pulse generator.
13. Observe a 0.1 volt square wave at pin #12 of Board #1.
14. Set Sensitivity to ÷ 1000.
15. Apply a 30 volt, peak-to-peak square wave from the pulse generator.

16. Observe a 30 MV peak-to-peak square wave at pin 12 of Board #1.

The Channel B attenuator is examined in exactly the same way, except, of course, the signal is applied to the Channal B, BNC connector, and Channel B controls are used. and the observation is made at pin 9 of board #1.

Straight Count Functional Check

To check the APTI-METER as a straight counter, proceed as follows:

1. Apply Power to APTI-METER.
2. Set Time Interval control to "1".
3. Set Channel A Trigger Slope Control.
4. Center Channel A Trigger Control to "+".
5. Set Channel A Sensitivity Switch to ÷100.
6. Set Display Time Control to mid-range.
7. Set Function Selector to FREQ. A.
8. Apply the following to the Channel A input BNC connector and observe Nixie readings shown:

INPUT	TIMER INTERNAL SETTING	DISPLAY
1 mc sinusoid	1 = (1 mc)	999,998 1,000,002*
from FREQ. STD. BNC	.1 = (100 kc)	100,000 ±1
"	.01 = (10 kc)	10,000 ±1
"	10^{-3} = (1 kc)	1,000 ±1
"	10^{-4} = (100 cps)	100 ±1
"	10^{-5} = (10 cps)	1 ±1

9. To check 10^{-6} position, set Display Time Control to MANUAL; observe that count starts by depressing Manual Reset push button and stops when push button is depressed a second time.

* NOTE: High reading will appear as 000,002.

Nixie Check

The purpose of this check is to determine that all numerals on each Nixie are operative. Proceed as follows:

1. Apply power to APTI-METER.
2. Set Time Interval Control to "1".
3. Set Channel A Trigger Slope Control to "1".
4. Center Channel A Trigger Level Control.
5. Set Channel A Sensitivity Switch to " ÷ 100".
6. Set Display Time Control to "MANUAL".
7. Set Function Selector to "FREQ. A".
8. With the inputs given below each numeral (0 – 9) on each Nixie should light, and only one numeral should ever appear on any Nixie:

INPUT FREQ.	CHECK NIXIE NO.
1 cps.	1
10 cps.	2
100 cps.	3
1 KC	4
10 KC	5
100 KC	6

Per. A Functional Check †

The following procedures check the APTI-METER's ability to measure the period of an input signal:

1. Apply power.
2. Set Time Interval Control as per following table.
3. Set Channel A Trigger Slope Control to "+".
4. Center Channel A Trigger Level Control.
5. Set Channel A Sensitivity Switch to "÷100".
6. Set Display Time Control to mid-range.
7. Set Function Selector Control to "PER. A".
8. Apply the following inputs, varying the Time Interval Control as shown to obtain Nixie readings given:

INPUT FREQ.	TIME INTERVAL SETTING	READ
1 mc	10^{-6}	1,000,001 ±1
100 KC	10^{-6}	10 ±1
10 KC	10^{-6}	100 ±1
1 KC	10^{-6}	1000 ±1
100 CPS.	10^{-6}	10,000 ±1
10 CPS.	10^{-6}	100,000 ±1
1 CPS.	10^{-6}	1,000,000 ±1
1 CPS.	10^{-5}	100,000 ±1
0.1 CPS.	10^{-4}	100,000 ±1

Period A to B Trigger Adjustments

For valid PERIOD A TO B measurements, it is necessary that the nixie readings obtained with the Function Selector Control in 'PERIOD A TO B' and 'FREQ A' positions be identical (with TRIGGER SLOPE CONTROLS for both Channels A and B set at the same slope). It is equally important that the sum (Step 7 below) of the two readings with the Trigger Slope (A and B) Controls at opposite positions (e.g. with A at "+" and B at "–") total the nixie reading obtained with the Function Selector at FREQ. A. To check, proceed as follows:

1. Apply power to APTI-METER.
2. Set Function Selector to PERIOD A TO B and Time Interval to "10^{-6}".
3. Set Sensitivity Switch (both channels) to "÷100".
4. Set Trigger Level (both channels) to mid-range.
5. Set A Channel Trigger Slope Control to "+".
6. Apply a 1 KC sine wave, 100 MV peak-to-peak, to the Channel A input.
7. Sum this input with the gate output at the rear pannel BNC and observe the result with an oscilloscope.
8. Vary Channel A Trigger Level control to check that the Trigger Level varies from the negative to the positive peak of the wave.
9. Check that Trigger Slope on "+" causes triggering on the positive input slope; and that triggering on the negative input slope occurs with the Trigger Level Control on "–".
10. Repeat 1 through 9 for Channel B.
11. Apply a non-symmetrical 1 KC square wave positive-going 100 μsec pulse at 200 MV, peak-to-peak, to both INPUT connectors.

† This check requires a frequency source at least as good as that of the frequency standard (see specifications), another Apti-Meter, or TSI Frequency Standard Model 566-R.

12. Set Function Selector to "PERIOD A TO B".
13. Set Time Interval to "10^{-6}".
14. Set Sensitivity Switch to "÷ 1".
15. Center both Channel Trigger Level Controls.
16. Obtain the following Nixie readings for the given Trigger Slope settings:

A-Slope	B-Slope	Approx. Reading
+	+	1000
−	−	1000
+	−	100
−	+	900

Period A X 10 Function Check

To check operation in this mode, proceed as follows;

1. Apply power to APTI-METER.
2. Set Channel A Trigger Slope to "+".
3. Center Channel A Trigger Level.
4. Set Channel A Sensitivity Switch to "÷100".
5. Center Display Time Control.
6. Set Function Selector to "PER. A."
7. Set Time Interval to "10^{-6}".
8. Apply 1 MC, to Channel A input.
9. Nixies should read 1 ±1.
10. Set Function Selector to "PER. A X 10".
11. Nixies should read 10 ±1.

Period A to B Functional Checks

To check functioning of the APTI-METER in this mode, proceed as follows:

1. Apply power to APTI-METER.
2. Set Function Selector to "PERIOD A TO B".
3. Set Time Interval to "10^{-6}".
4. Center Display Time Control.
5. Set Channel A Trigger Slope to "+" and B Trigger. Slope to "−".
6. Set both Sensitivity Switches to "÷100".
7. Apply an approximately square-wave, 100 KC signal at approximately 6V, peak-to-peak to both INPUT connectors.
8. Adjust both Trigger Level Controls to obtain reading of 5 ±1.
9. Nixies should read 5 ±1 and should hold this reading over approximately 90 ° variation of either Trigger Level Control.
10. Repeat this procedure with A Trigger Slope at "−" and B Trigger Slope at "+" observing the same result. With both Trigger Slope Switches at "+" or "−" the reading will be 10 ±1.
11. Disconnect 100 KC signal and apply 1 KC repetition rate pulse at 5V, peak-to-peak. Begin with pulse width of 100 μsec and vary down to 0.1 μsec to determine that period measurement is accurate for each setting of pulse generator pulse width.

Ratio B/A Functional Check

To Check operation in this mode, proceed as follows:

1. Apply power to APTI-METER.
2. Set Function Selector to RATIO B/A.
3. Set Time Interval to "1".
4. Center Display Time and both Trigger Level Controls.
5. Set both Sensitivity Switches to "÷100"-
6. Set Channel A Trigger Slope to "+" and Channel B Trigger Slope to "−".
7. Apply 1 MC, 5V pulse to Channel B.
8. Apply 1 CPS, 5V pulse to Channel A.
9. Reading on Nixies should be approximately 1,000,000.
10. Decrease 1 MC toward 1 CPS. on Channel B input.
11. Nixies should read decreasingly as 1MC is decreased.

Location of Faulty Board

If the functional checks, tests, and adjustments preceding and in Section VI do not indicate proper functioning of the APTI-METER, it is necessary to isolate the board or chassis-mounted component at fault. It is emphasized that a thorough familiarity with Sections IV and V will permit ready location of the probable fault as indicated by the preceding discussions. The measurements immediately following should be used to confirm the analysis and cannot by-pass it without the loss of much time. Every attempt should be made to determine trouble sources by front panel indication before proceeding with more elaborate trouble shooting.

If, in proceeding with the measurements given, it is found that the input to the board is as shown but one or more of outputs is not in agreement, it reasonable to assume that the board is malfunctioning. This assumption should be verified by making power supply checks, visual inspection of the instrument, inspection and cleaning of contacts, etc. A board of the same type should be used to replace the suspect board and the functional checks made after all adjustments and calibrations have been accomplished.

Board No. 1 - Input Amplifiers, 1CPS and 0.1 CPS Time Base Generators

At pin#	Observe/Measure	If NO, Check
19	-10VDC	Power Supply
10	- 9VDC	Power Supply
8, 13, 18	Ground	Open
3	10cps, Approx. Square Wave 5V, p-p	Board #10, Pin 2
1	0.1cps, Approx. Square Wave, 5V, p-p	Board #1 faulty
2	1 cps Approx. Square Wave 5V, p-p	Board #1 faulty
4	See Waveforms	Board #1, pin 9
6	See Waveforms	Board #1, pins 9, 4
7	See Waveforms	Board #1, pins 9, 4

9	Input waveform (B)	Channel B attenuator & BNC connector
3	Input Waveforms (A)	Channel A attenuator & BNC connector
14	*	Board #1, pins 12, 17
15	*	Board #1, pins 12, 17
17	*	Board #1, pin 12

Board #2 Gate and Display Logic

At pin#	Observe/Measure	If NO, Check
15	-10 VDC	Power Supply
11,13,17	Ground	Open
19	1MC Sine Wave, 100KC 1KC, 100CPS, 10CPS, or 0.1CPS square wave	Check xtal osc. Brd. #10, Time Interval SW
2	*	Faulty Board
10	1KC square wave, 5V p-p (min); use 4.7K load	Pin 9 of Board #2
9	*	Pin 4 of Board #4
8	*	Faulty Board
1	*	Faulty Board
5	-10VDC (with MANUAL RESET depressed)	MANUAL RESET Switch; Power Supply
6	-10V (with MANUAL TIMING depressed)	MANUAL TIMING Switch; Power Supply

Board #3; Signal Divider

At pin#	Observe/Measure	If NO, Check
1	*	Board #1, pins 14 or 15
2	*	Board #1, pins 14 or 15
3	*	Board #1, pins 6 or 7
16	*	Board #1, pins 6 or 7
8	Observe Pin 16 Waveform X 10	Faulty Board
11	5V (min) p-p 1mc sine wave across 4.7 K load	xtal oscillator if OK Faulty board
12	With Time Interval at 10^{-6} observe 1mc sine wave	xtal oscillator
13	Observe 5V, p-p sine wave with pin 12 as stated	xtal oscillator Faulty board
15	-10VDC	Power Supply
17	GND	Open

Boards 4, 5, 6, 7– 100 KC Counters (see Note 2)

At pin#	Observe/Measure	If NO, Check
1 (5)	-10VDC	Power Supply
2 (3)	Ground	Open
3 (6)	Reset pulse;*	Pin 8 of board #2
4 (4)	Output Trigger;*	Pins 6, 7, or 14, 15 of Board #1; Pin 16 of Board #2
5 (1)	Square wave, 4V, peak to peak	Pin 16 of Board #2
6 (11)	Nixie cathode No. 1*	Pin #5
7 (9)	Nixie cathode No. 3*	Pin #5
8 (8)	Nixie cathode No. 4*	Pin #5
9 (7)	+300 VDC	Power Supply
10 (14)	Nixie cathode No. 5*	Pin #5
14 (16)	Nixie cathode No. 7*	Pin #5
15 (15)	Nixie cathode No. 6*	Pin #5
16 (12)	Nixie cathode No. 0*	Pin #5
17 (17)	Nixie cathode No. 8*	Pin #5
18 (18)	Nixie cathode No. 9*	Pin #5
19 (10)	Nixie cathode No. 2*	Pin #5

Board #8, 100 KC Fast Counter (see Note 2)
(Identical to Boards 4, 5, 6, 7)

Board #9, 1MC Counter
(Identical to Boards 4, 5, 6, 7) (see Note 2)

Board #10 Time Base Generator

At pin#	Observe-Measure	If NO, Check
1	10 CPS, sq. wave, 8V, peak to peak	Pin #19; oscillator
2	10 CPS, sq. wave, -5V, peak to peak	Pin #19; Faulty board
3	-10VDC	Power Supply
4	100 CPS sq. wave, -5V, peak to peak	Pin #19; Faulty board
5	1KC*	Pin #19; Faulty board
14	Ground	Open
15	10KC sq. wave -5V, peak to peak.	Pin #19; Faulty board
16	100KC, sq. wave, 8v, peak to peak	Pin #19; Faulty board
18	1mc sine wave	Oscillator
19	1mc sine wave	Oscillator

*Note 1: See Waveforms, page 7-10.
Note 2: In APTI-METERS with serial numbers below No. 312, decade counter pin numbers are those shown in parentheses.

Input Channel Attenuator Adjustments

The attenuators corresponding to settings of the SENSITIVITY SWITCHES include provision for adjustment by means of ceramic trimmer capacitors which are part of the attenuator networks. There are eight trimmer capacitors located behind the front panel of the unit; four are associated with the Channel A SENSITIVITY Switch and four are associated with that of Channel B. These are shown in the photograph of the front panel. To adjust the attenuators for proper attenuation proceed as follows:

1. Apply power to Apti-Meter.
2. Apply a 1KC square wave to Channel A INPUT BNC, of 0.1 volts amplitude.
3. Set Channel A SENSITIVITY Switch to +1.
4. Observe the pulse at collector of Q11, Board #1 and adjust Ch. A ÷ 1 capacitor for flat-top pulse shape.
5. Set SENSITIVITY to ÷ 10 and adjust Ch. ÷ 10 capacitor for flat-top pulse shape at collector of Q11 Board #1.
6. Apply a 10 volt pulse; Set SENSITIVITY to ÷ 100.
7. Observe flat-top pulse at collector of Q11, Board #1 and adjust capacitor Ch. A ÷ 100 as required.
8. Apply a 30 volt pulse. Set SENSITIVITY to ÷ 1000. Observe pulse at collector of Q11, Board #1 and adjust capacitor Ch. A ÷ 1000 as required.
9. Apply pulses as above sequentially to Channel B input connector. Pulses should be observed at the collector of Q3, Board #1.

The locations of the attenuator capacitors and the switch settings associated with each for each channel are as follows:

SENSITIVITY SWITCH SETTING	CAPACITOR & LOCATION
Ch. A ÷ 1	Front, bottom*
Ch. A ÷ 10	Rear, bottom*
Ch. A ÷ 100	Rear, Center*
Ch. A ÷ 1000	Uppermost*
Ch. B ÷ 1	Front, bottom**
Ch. B ÷ 10	Rear, bottom**
Ch. B ÷ 100	Rear, center**
Ch. B ÷ 1000	Uppermost**

*Behind Channel A Controls
**Behind Channel B Controls

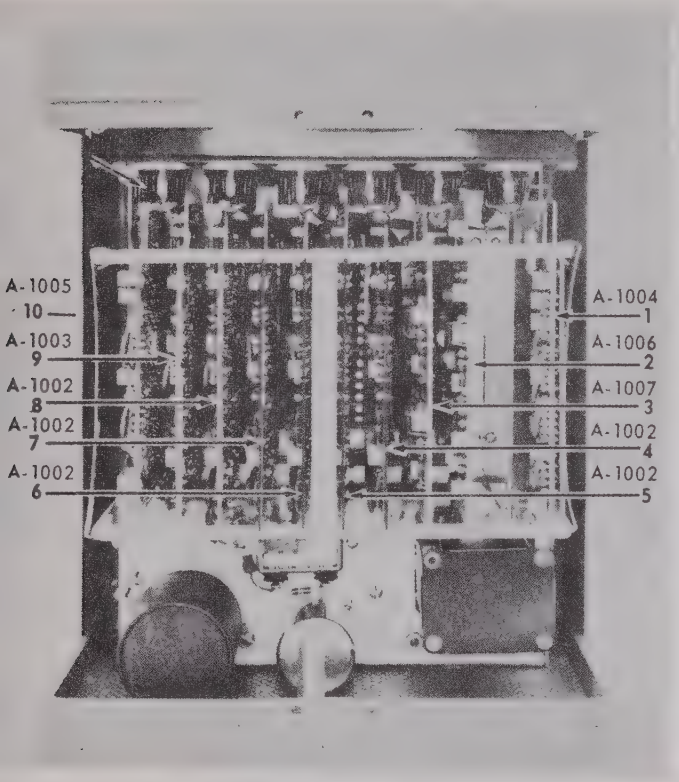
(see addendum for rack mount attenuator locations)

Time Base Trimpot Adjustments

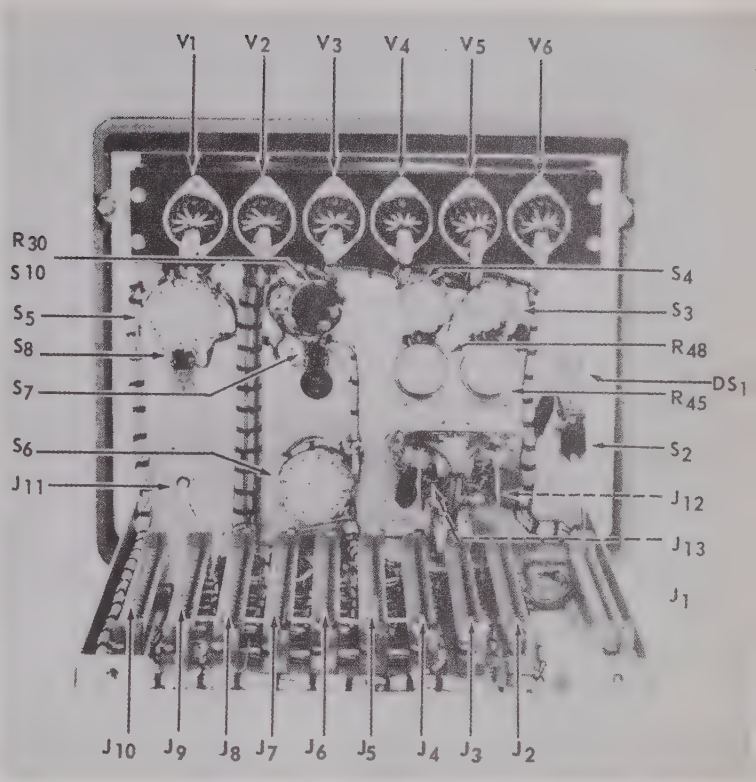
It may become necessary occasionally to adjust the Apti-Meter time bases. This necessity will manifest itself as an incorrect reading in one or more time base positions during test; the nixie reading may begin with an 8 or 12 rather than the normal 10. This is adjusted by varying the appropriate trimpot. If the nixie reading is low the trimpot should be adjusted clockwise using a thin-bladed screwdriver; if the reading is high a counterclockwise adjustment should be made. Observe the display for the proper nixie reading as the adjustment is made. The range of adjustment of the trimpot is 25 turns end to end. The following table associates the appropriate trimpot with the corresponding setting of the TIME INTERVAL switch. Adjust trimpot to center of correct reading range.

SWITCH SETTING	TRIMPOT & LOCATION
10^{-6}	none
10^{-5}	1st trimpot from front board #10
10^{-4}	2nd trimpot board #10
10^{-3}	3rd trimpot, board #10
.01	4th trimpot, board #10
.1	5th trimpot, board #10
1 second	trimpot at rear of board #1
10 seconds	trimpot at front of board #1

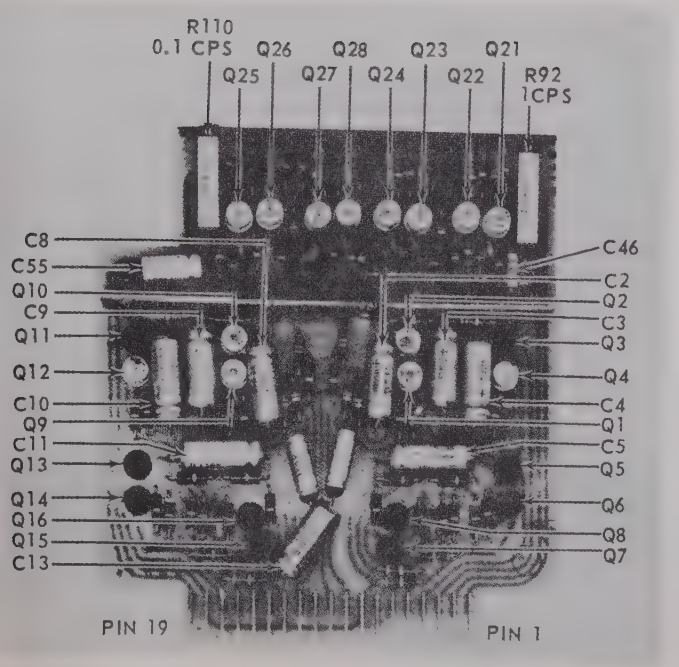
(see addendum for rack mount trimmer locations)



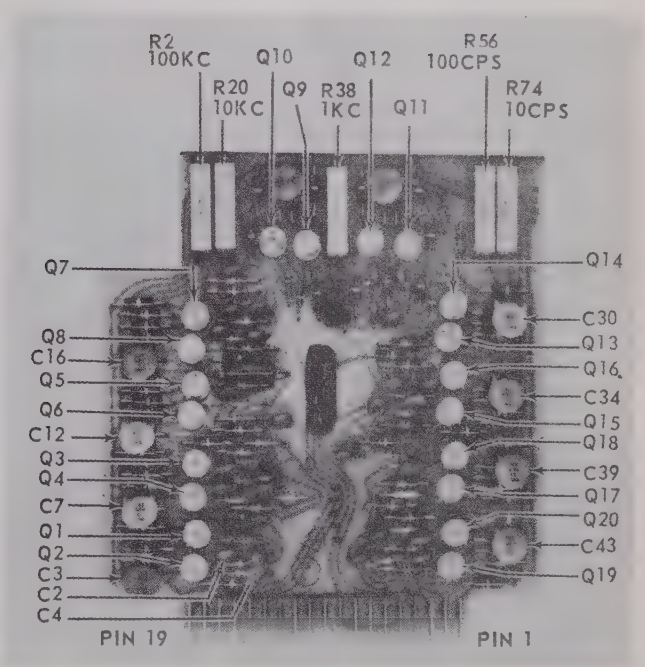
ASSEMBLED APTIMETER
(Top View)



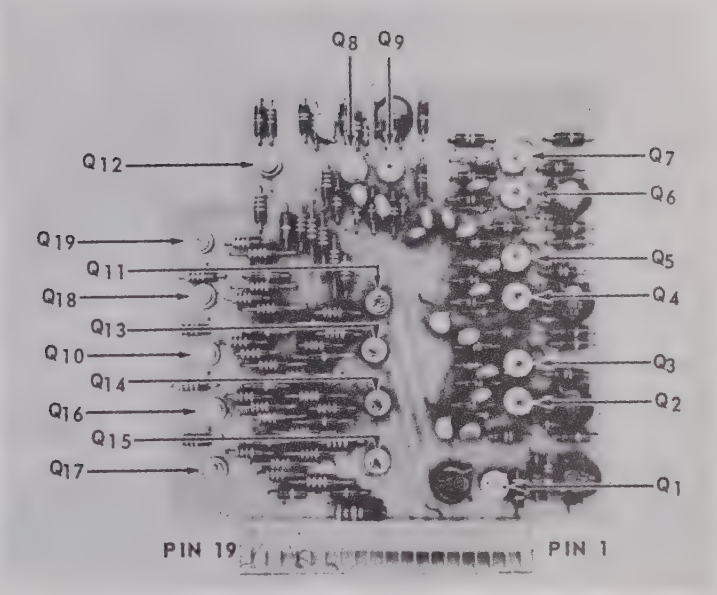
APTI-METER FRONT PANEL
(Rear View)



"B" BOARD SCHEMATIC 609D103

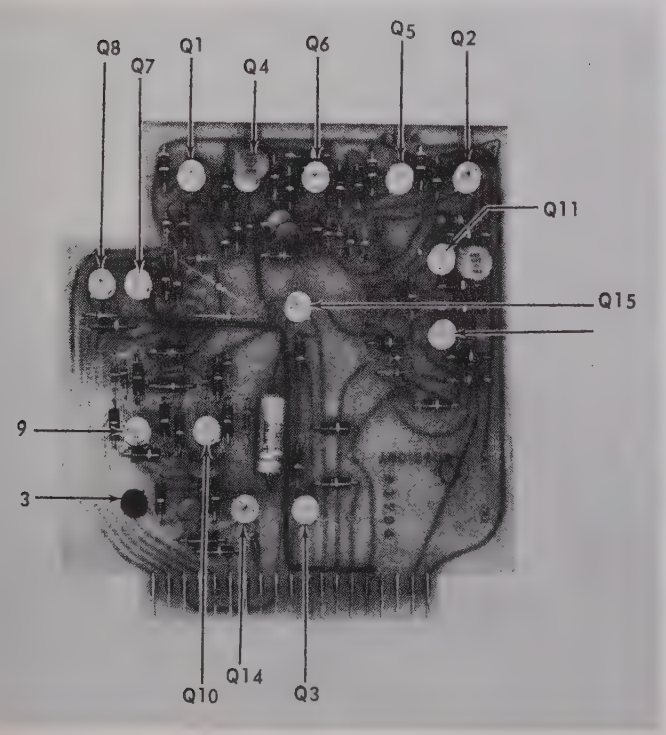


"C" BOARD SCHEMATIC 609D104

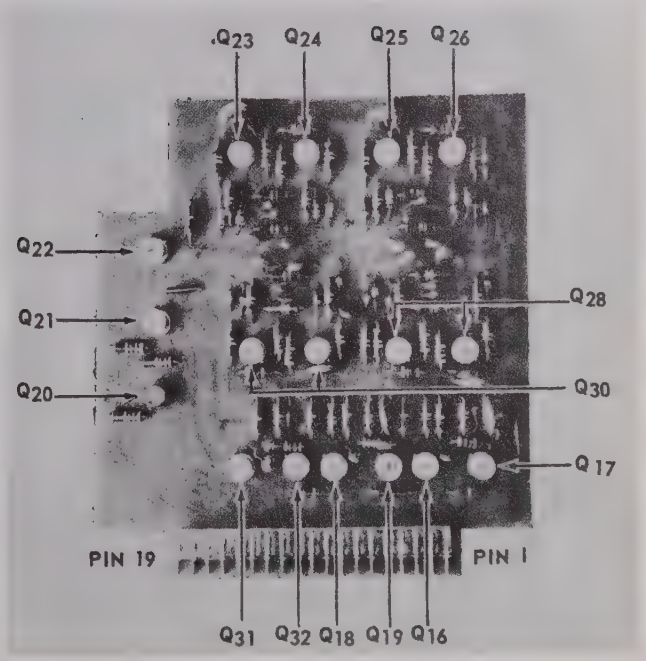


"A" BOARD SCHEMATIC 609D102, 106, 107

used in units after serial #310 and all rack mount units.

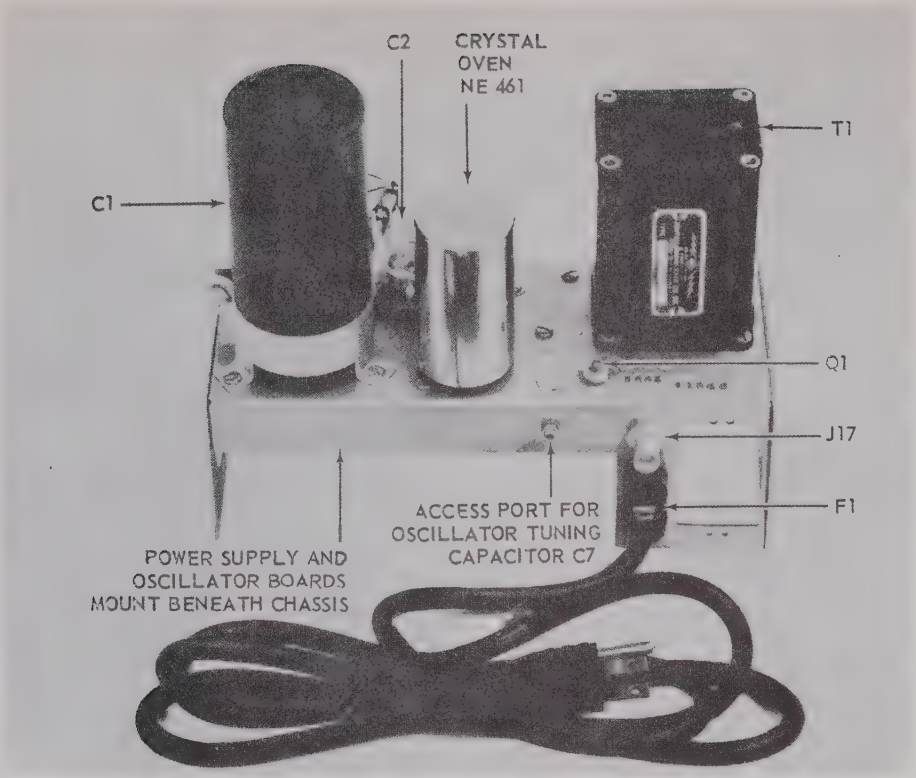


"D" BOARD SCHEMATIC 609D105A



"E" BOARD SCHEMATIC 609D105

Figure 7–1 APTI-METER – Parts Location



POWER SUPPLY AND 1MC OSCILLATOR SCHEMATIC 609D130

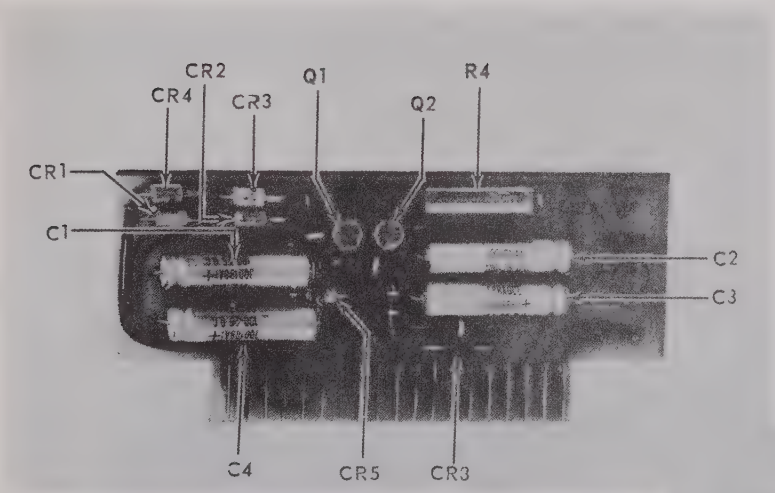


FIGURE C.
POWER SUPPLY BOARD.

FIGURE D.
OSCILLATOR BOARD

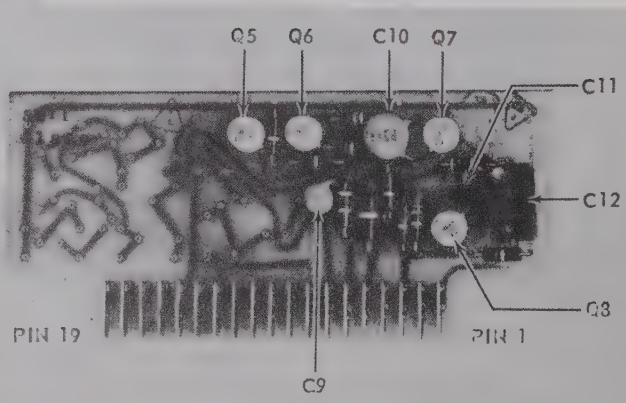


Figure 7-2 Power Supply and 1MC Oscillator – Parts Location

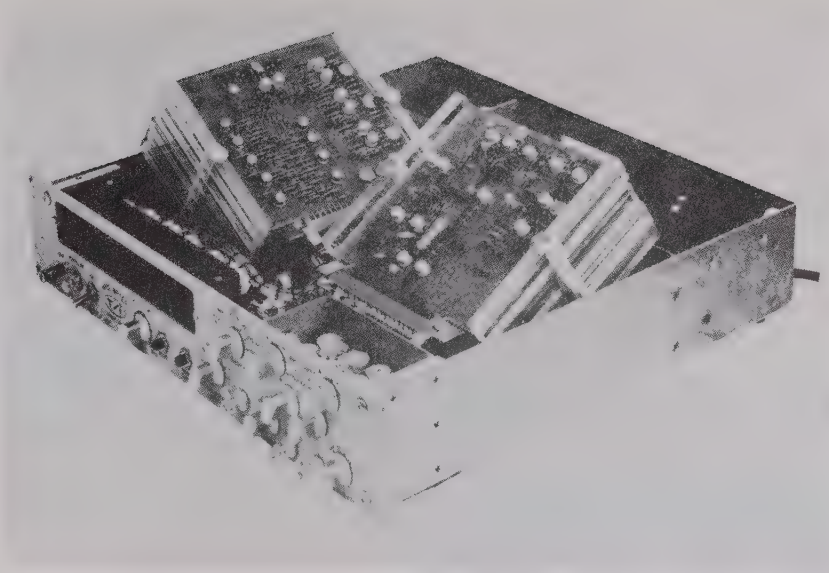


FIGURE A. MODEL 361-R APTI-METER BOARDS TILTED & LOCKED IN POSITION FOR SERVICING.

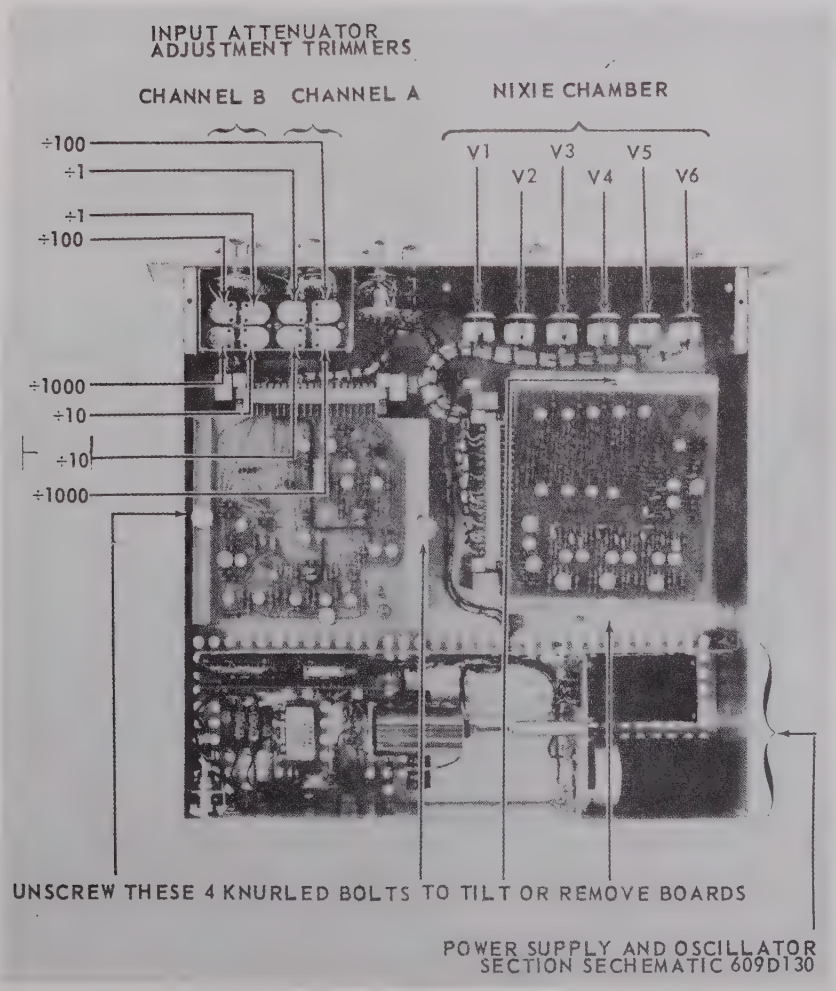


FIGURE B. MODEL 361-R APTI-METER TOP VIEW

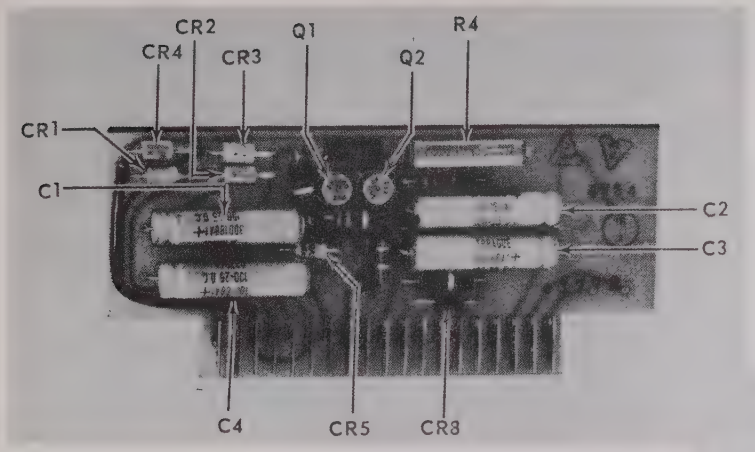
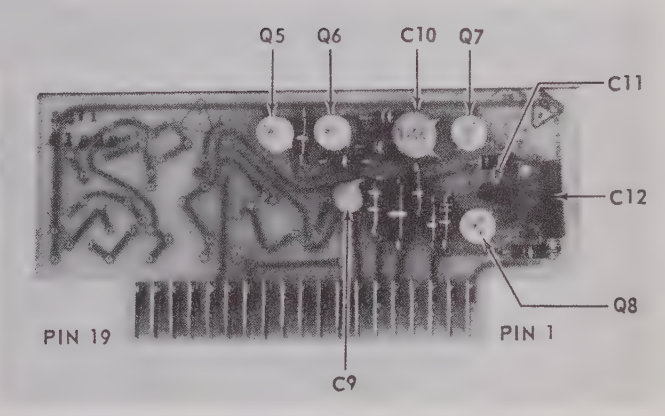


FIGURE C.
POWER SUPPLY BOARD.

FIGURE D.
OSCILLATOR BOARD



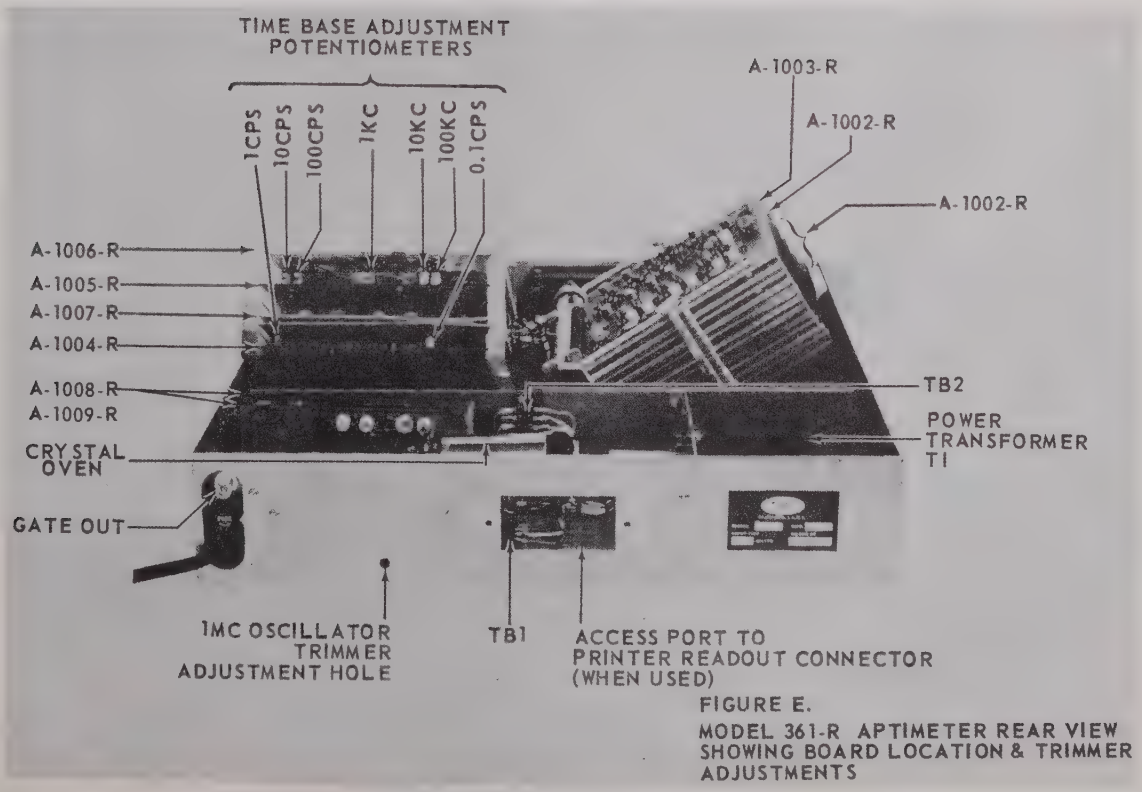


FIGURE E.
MODEL 361-R APTIMETER REAR VIEW SHOWING BOARD LOCATION & TRIMMER ADJUSTMENTS

Figure 7-3 Rack Model APTI-METER – Parts Location

BOARD #4, 5, 6, 7, 8, 9-DECADE READOUT (609-D-106, 609-D-107)

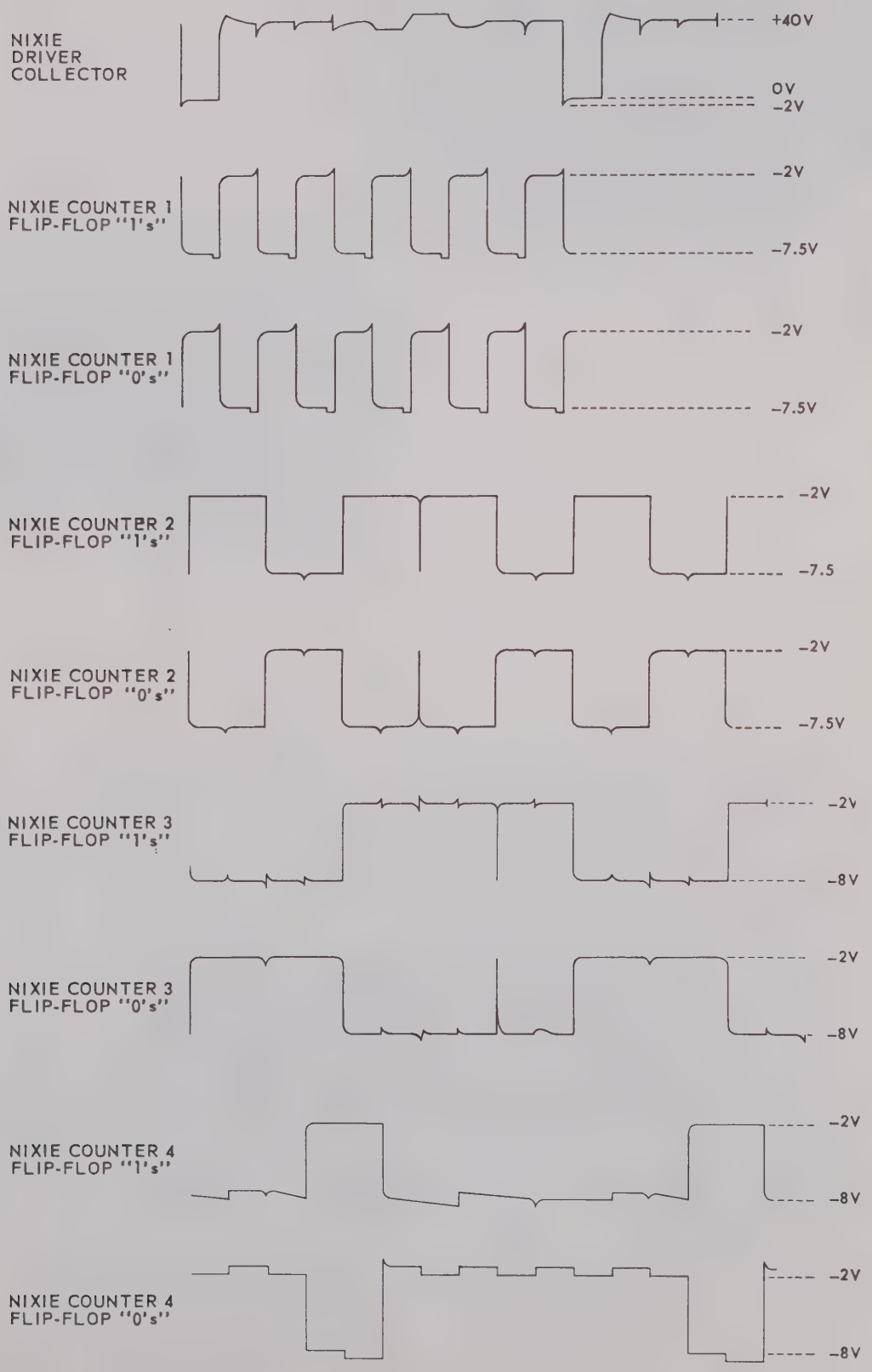
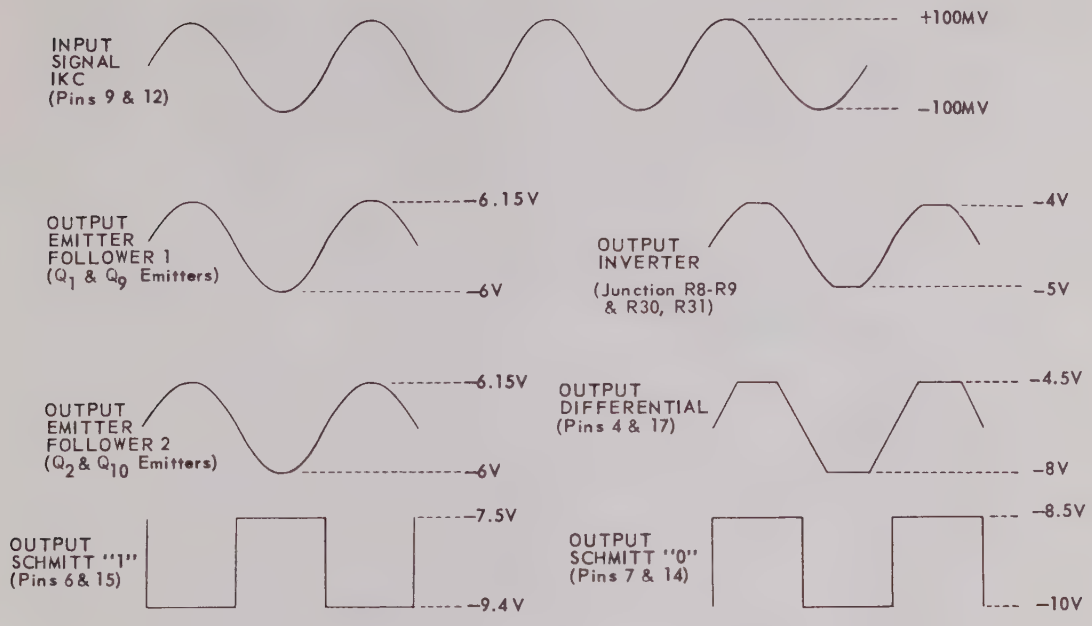


Figure 7-4 A Waveforms

BOARD # 1 INPUT AMPLIFIER (SCHEMATIC 609-D-103)



BOARD # 10 TIME BASE GENERATOR (SCHEMATIC # 609-D-104)

BOARD # 2 GATING LOGIC (SCHEMATIC 609-D-191)

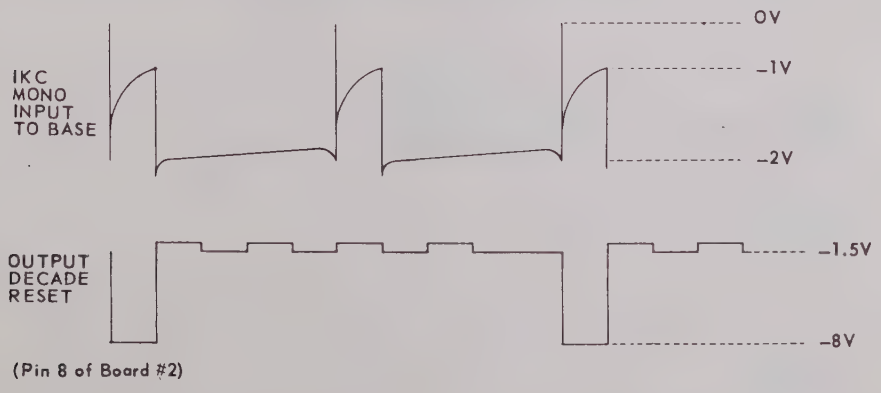
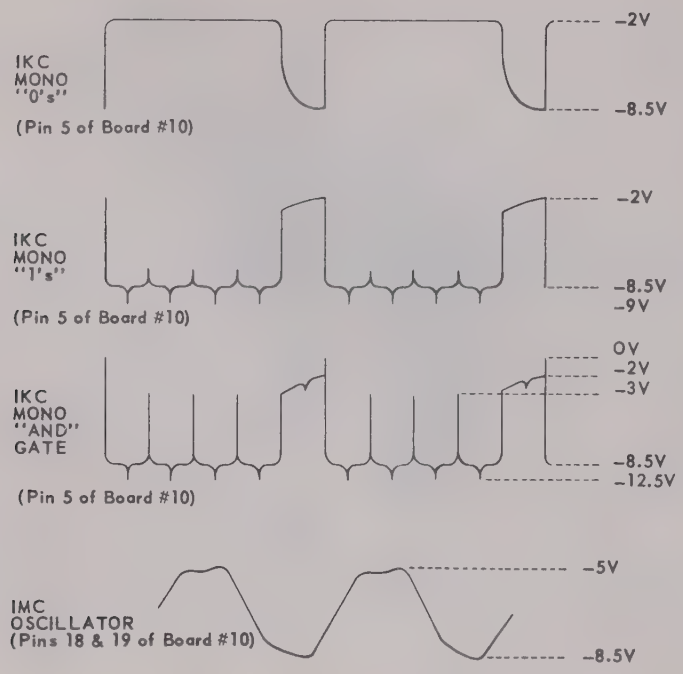


Figure 7-4B Waveforms

BOARD # 10 TIME BASE GENERATOR (SCHEMATIC 609-D-104)



BOARD # 2 GATING LOGIC (SCHEMATIC 609-D-191)

BOARD # 3 SIGNAL DIVIDER (SCHEMATIC 609-D-195)

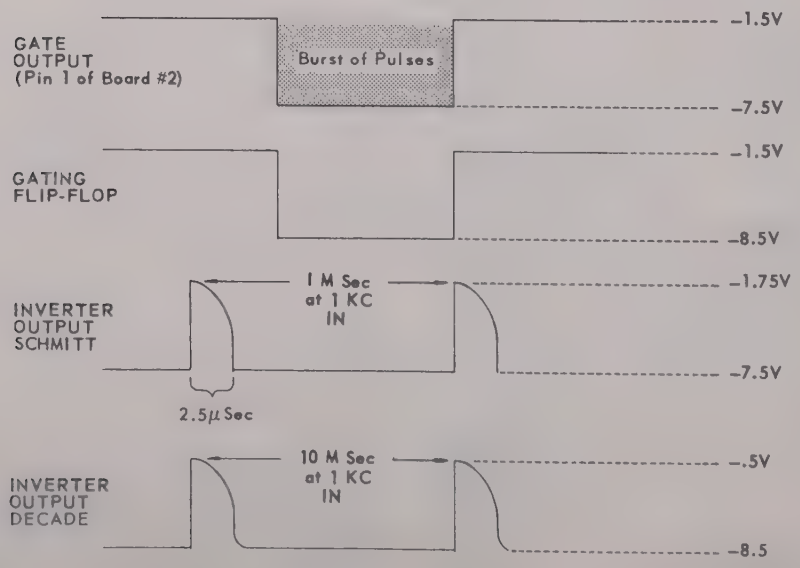
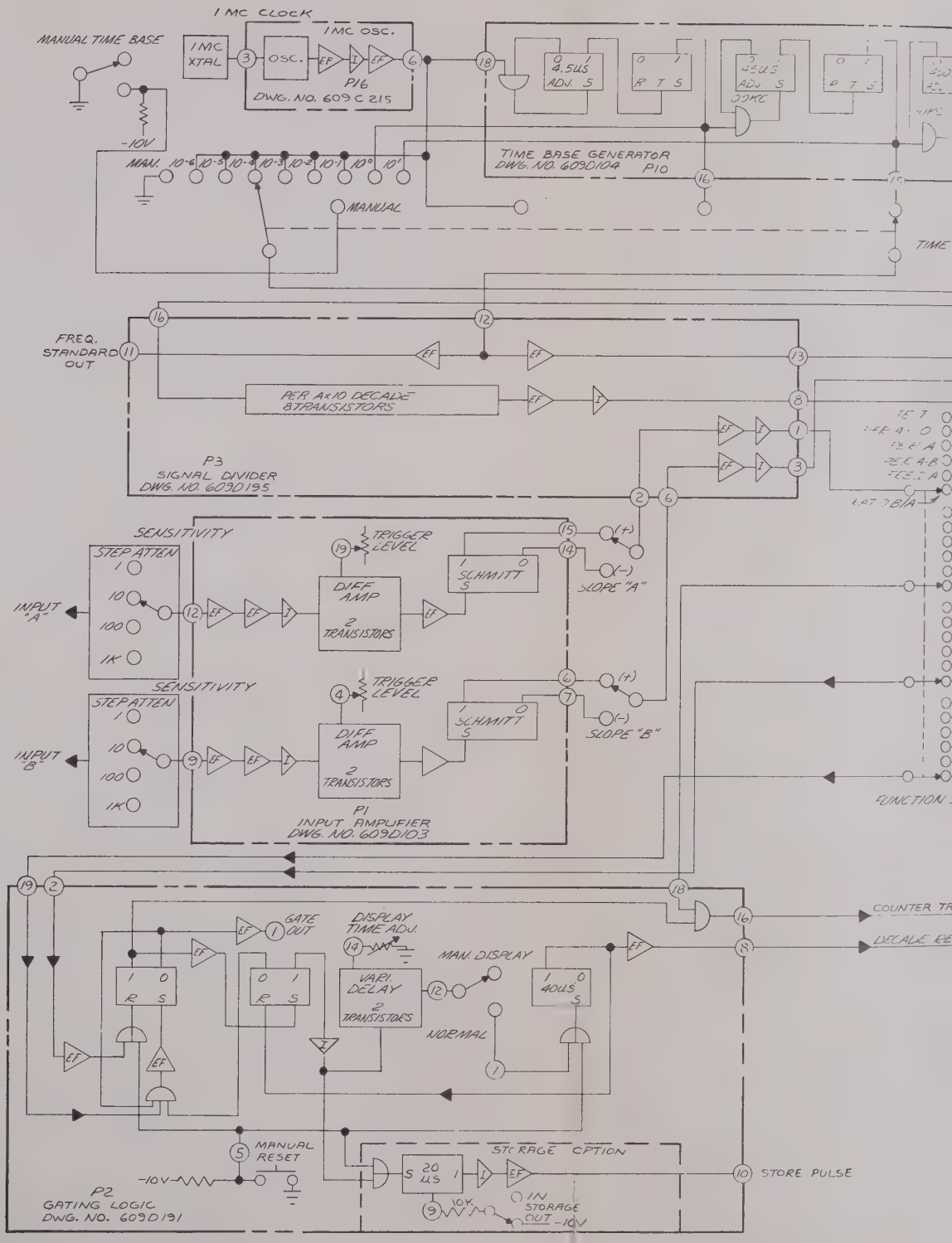
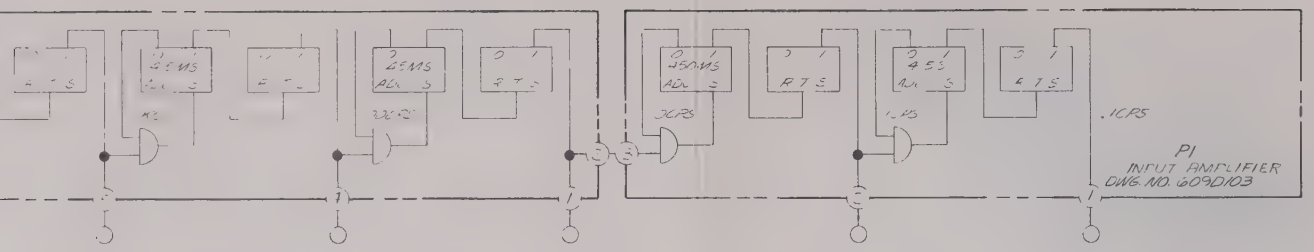
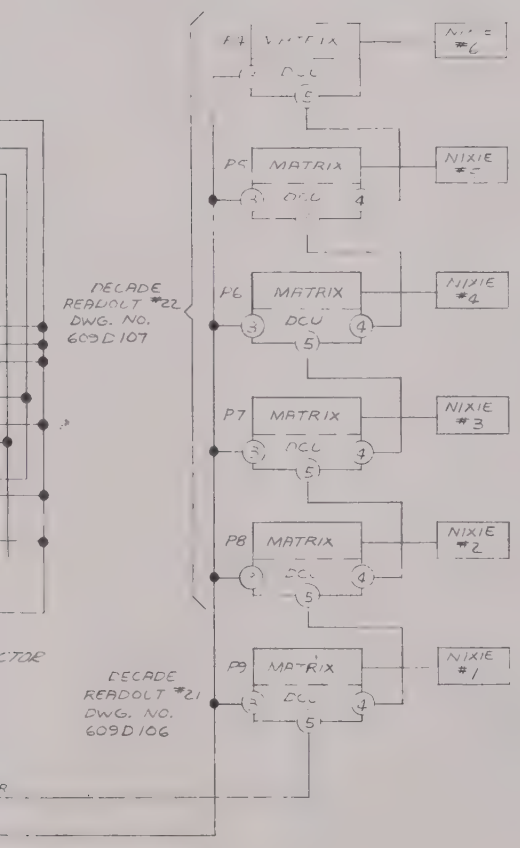


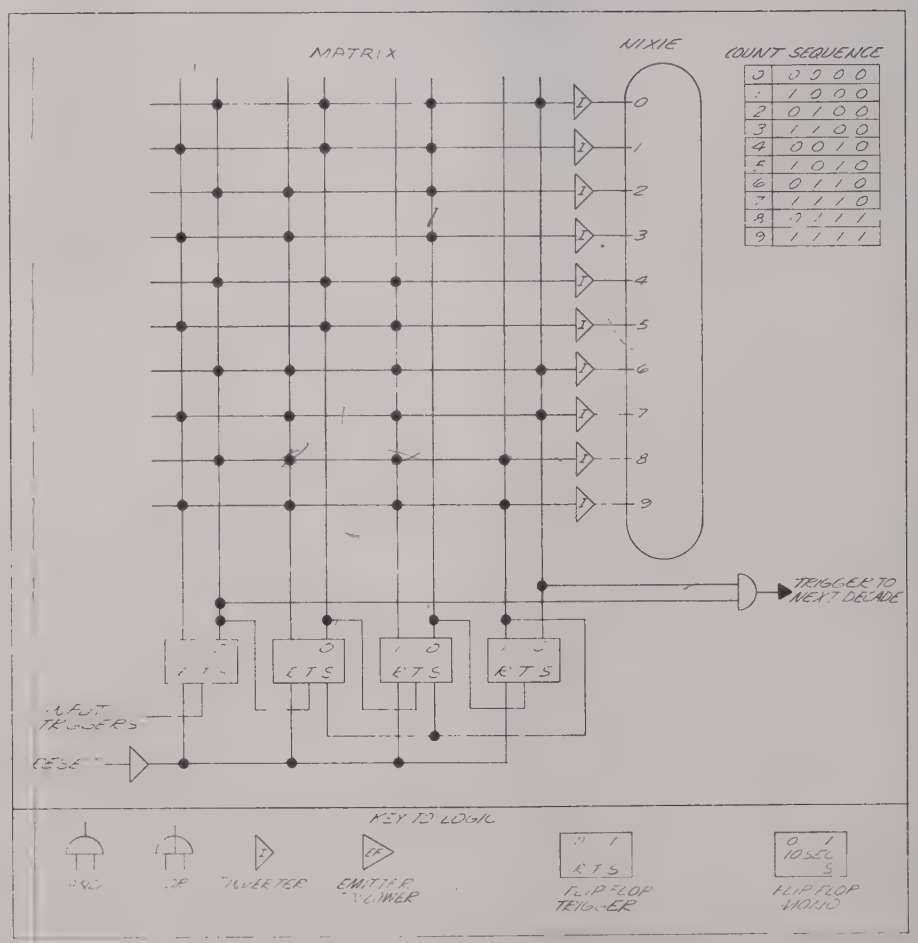
Figure 7-4C Waveforms


1 MC CLOCK
1 MC OSC.
MANUAL TIME BASE
1 MC XTAL
OSC.
P16
DWG. NO. 609C215
-10V
MAN. 10-6 10-5 10-4 10-3 10-2 10-1 10° 10¹
TIME BASE GENERATOR
DWG. NO. 609D104 P10
MANUAL
FREQ. STANDARD OUT
PER AX10 DECADE 8 TRANSISTORS
P3
SIGNAL DIVIDER
DWG. NO. 609D195
SENSITIVITY
STEP ATTEN
1
10
100
1K
INPUT "A"
INPUT "B"
TRIGGER LEVEL
DIFF AMP
2 TRANSISTORS
SCHMITT
SLOPE "A"
SLOPE "B"
P1
INPUT AMPLIFIER
DWG. NO. 609D103
GATE OUT
DISPLAY TIME ADJ.
VARI DELAY
2 TRANSISTORS
MAN. DISPLAY
NORMAL
MANUAL RESET
STORAGE OPTION
STORE PULSE
IN STORAGE OUT
P2
GATING LOGIC
DWG. NO. 609D191

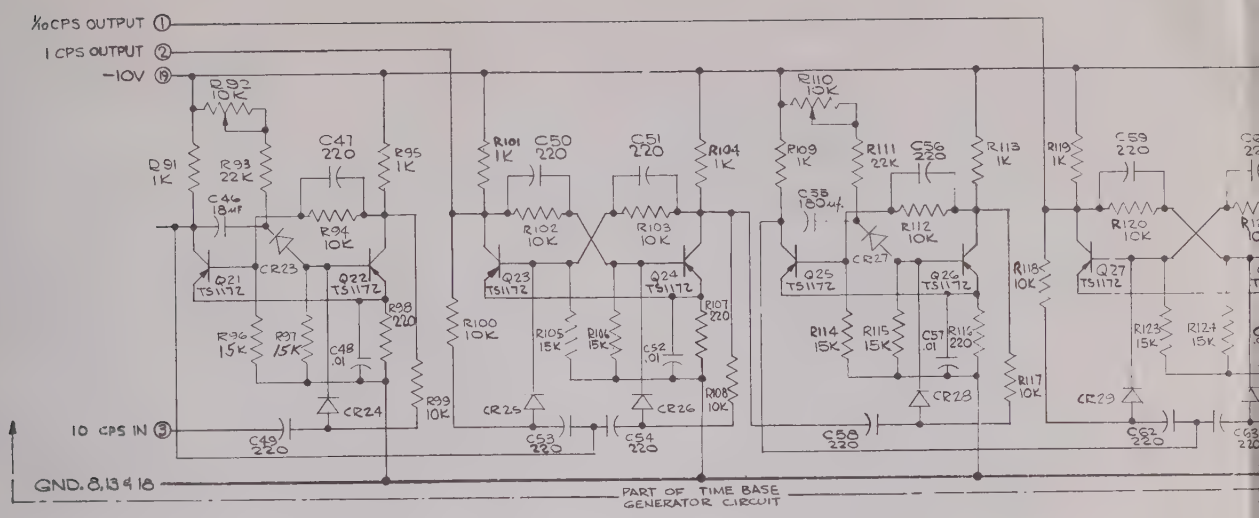


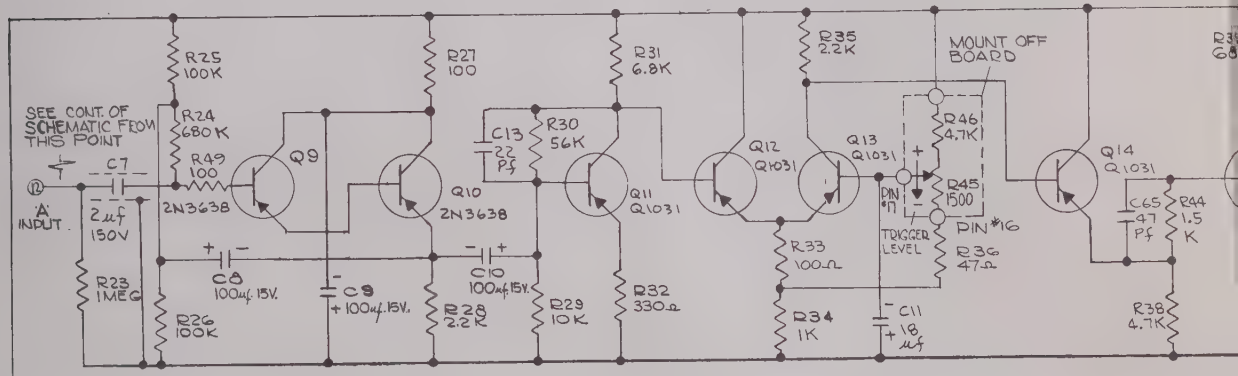
SELECTION



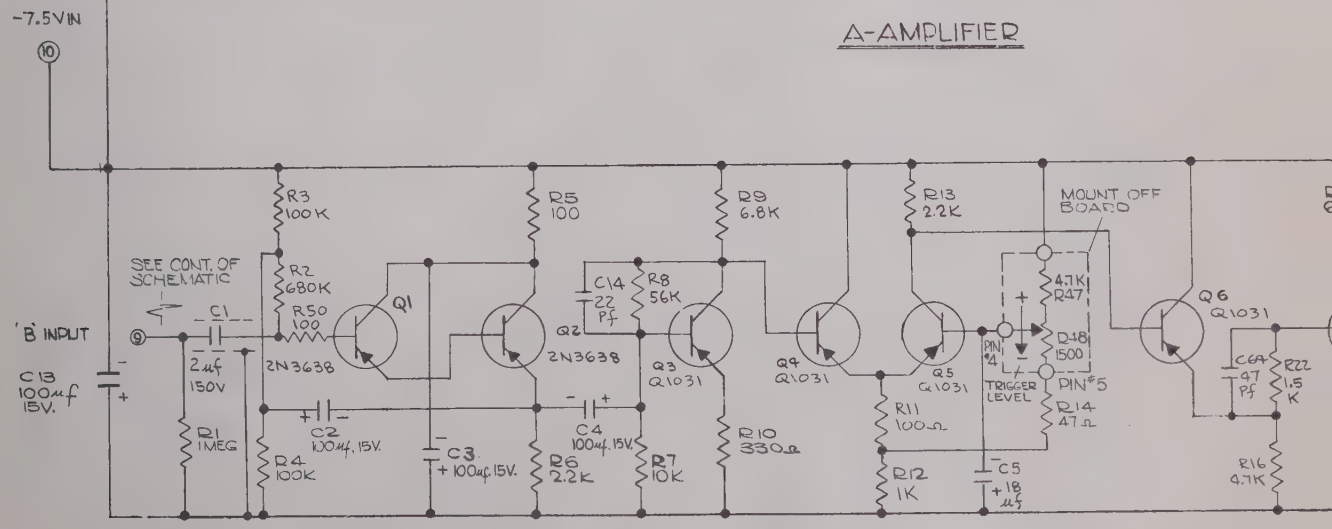


TITLE: LOGIC DIAGRAM	ASSOCIATED DRAWINGS	
	DRAWN R.W.	DATE 10-8-62
	CHKD	609E156
TRANSISTOR SPECIALTIES, INC.	APPR	REV B





A-AMPLIFIER



B-AMPLIFIER

NOTE: 1- ALL DIODES IN191 UNLESS OTHERWISE SPECIFIED.
2- ADD COPPER LAMINATE SHIELD 1/2 x 5 3/4 BETWEEN COUNT DOWN AND AMPLIFIER PORTION OF BOARD. ATTACH TO BOARD GROUND.
3- ADD 6" x 5 3/8 NOTCHED LAMINATE SHIELD ON SPACES (CERAMIC) ON DIP SIDE. GROUND TO PIN #13.

6- USE TS1172 (OR EQUIV.)
7- USE 2N1754 (OR EQUIV.)

N°	REVISION	DATE
'A'	VALUES ADDED TO COMPONENTS. REDESIGN FRONT PANEL. PINS SHOWN	AUG 3.60
'B'	Q1, 2, 9 & 10 WAS 2N1499 AS PER ECO # EE9	AUG 22.60
'C'	ADD NOTE #2, 3, 4 & 5. R39 AND R17 WAS 2.2K. R42 AND R20 WAS 680. R19 AND R21 WAS 470. R18 AND R40 WAS 6.8K. REMOVED R15 AND R27 (6). C6 AND C12 WAS 47PF. REMOVED C9, 14 & CR2. REMOVED R49 (47K) AS PER ECO # 8	AUG. 29. 60
'D'	Q 4 AND Q12 WAS 2N1499 AS PER ECO # EE10	SEPT. 1. 60
'E'	ADDED C14 & C15 DISC. CERM. CAPS ECO # 21	NOV. 1. 60
F	DELEATED C14, & C15 ECO. # 260	9-29-61
G	AS PER ECO # 280	7-1-62 EW
H	AS PER ECO # 447	7-7-63
J	AS PER ECO # 726	6-21-65
K	AS PER ECO # 754	8-19-65
L	AS PER ECO # 801	9-26-67
M	AS PER ECO # 832	8-14-65
N	AS PER ECO # 955	11-11-65
P	AS PER ECO # 981	11-1-66
Q	AS PER ECO # 1019	11-30-66
R	AS PER ECO # 1039	1-11-67
S	AS PER ECO # 1040	1-11-67

ON FRONT PANEL

8-10" COAX

INPUT A

1M

47pf

÷ 1

7-45 Pf.

÷ 10

7-45 Pf.

47K

330 pf

÷ 100

7-45 Pf.

4.7K

3300pf

÷ 1000

7-45 Pf.

470

.03 uf.

GND.

INPUT B

GND. TO CHASSIS AT PANEL

NOTE: INPUT 'A' OR 'B' IDENTICAL

NOTE: THIS IS A CONTINUATION OF SCHEMATIC FROM POINT INDICATED.

R122 1K

R125 220

R126 10K

R42 470

ZEROS OUT

OUTPUT 'A' SCHMITT

ONES OUT

C12 47 Pf

R40 1K

Q15 Q1031

Q16 Q1031

R41 1K

R43 10K

R20 470

ZEROS OUT

ONES OUT

OUTPUT 'B' SCHMITT

C5 47 Pf

R18 1K

Q8 Q1031

R19 1K

R21 10K

ASSOCIATED DRAWINGS

TITLE: INPUT AMPLIFIER "B" BOARD

TRANSISTOR SPECIALTIES, INC

DRAWN SCL

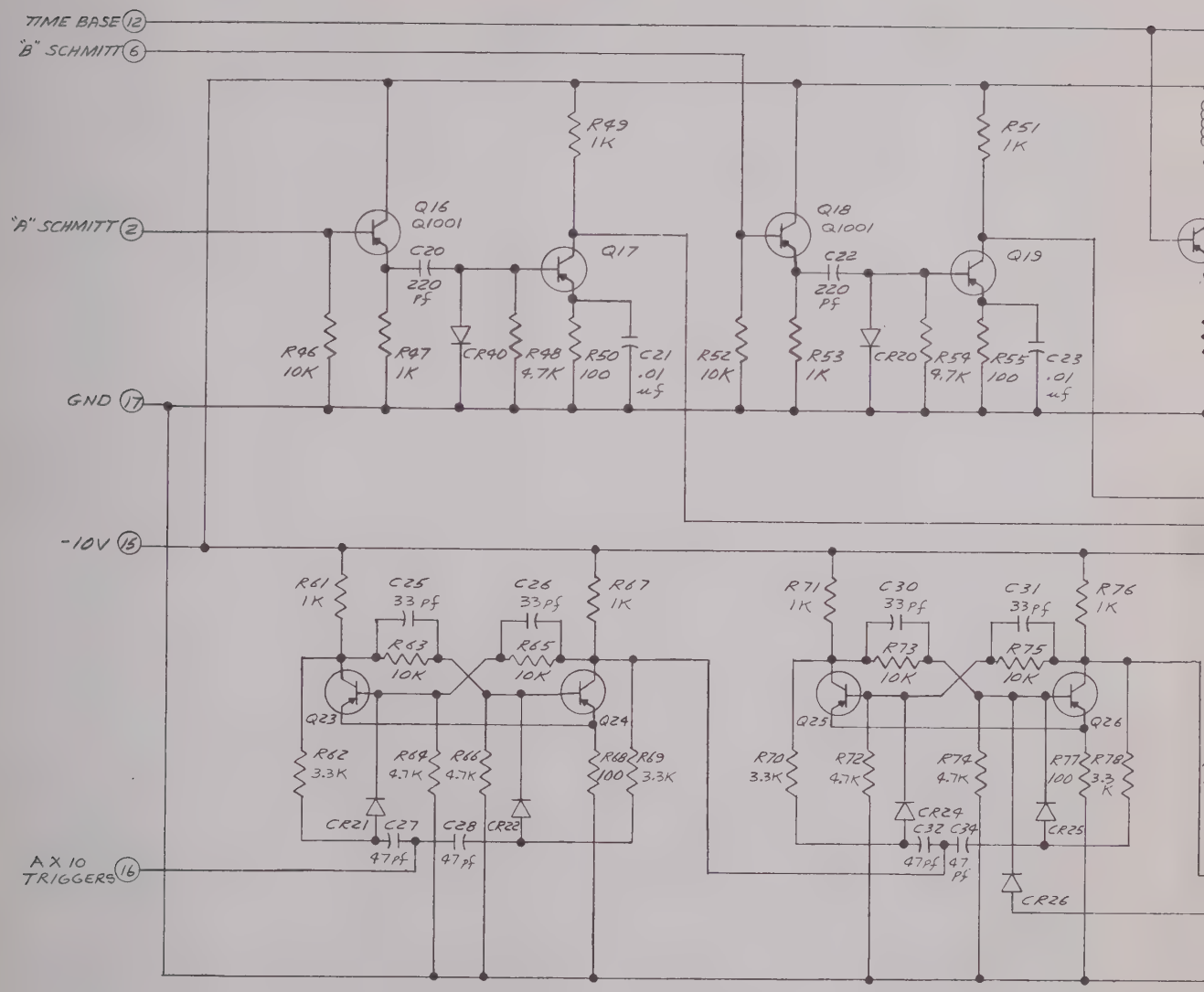
CHK'D

APPR'D

DATE 5/18/60

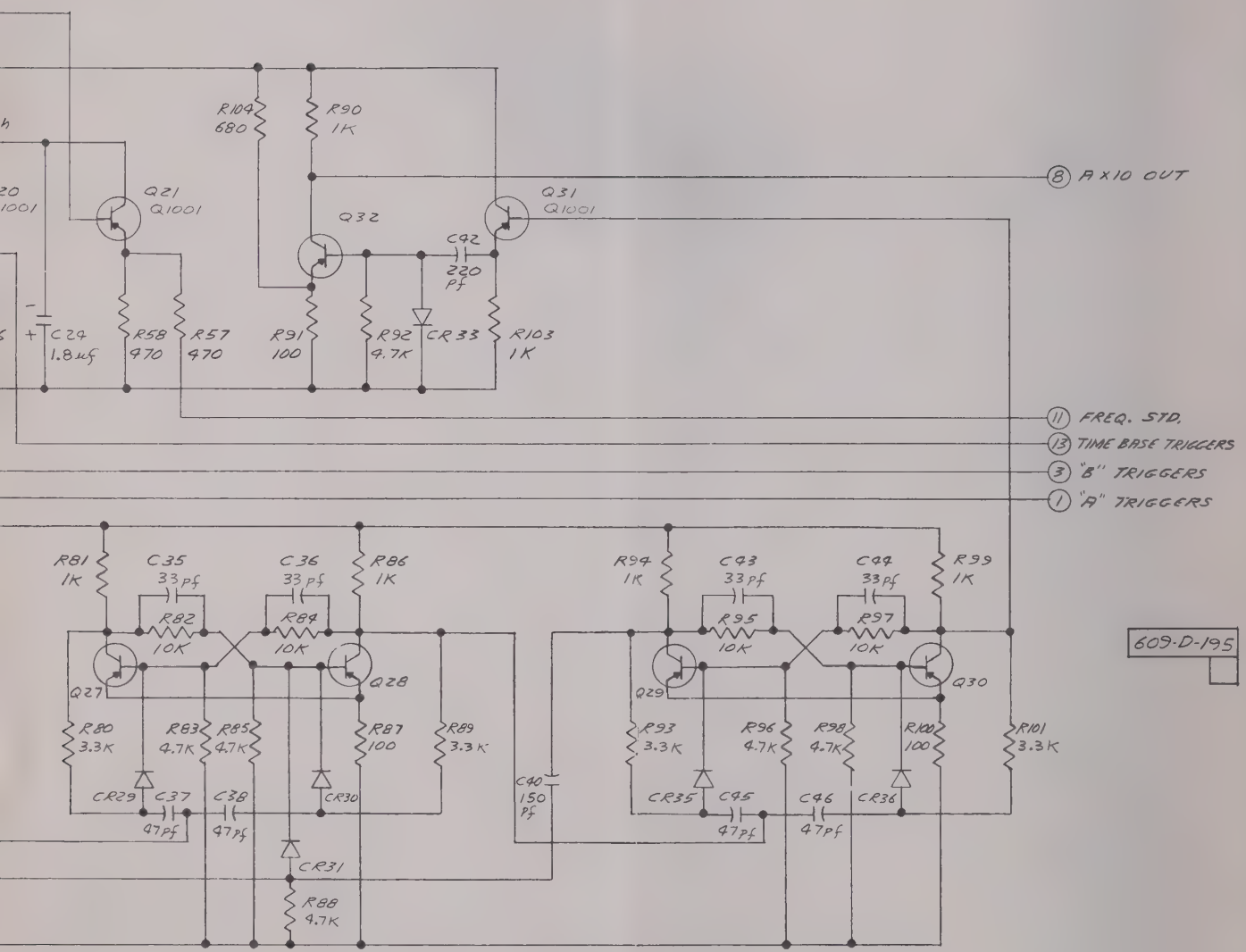
609 D 103

REVISION S



NOTES:

1. ALL TRANSISTORS ARE
2. ALL DIODES ARE
3. PRINTED CKT. BD. #



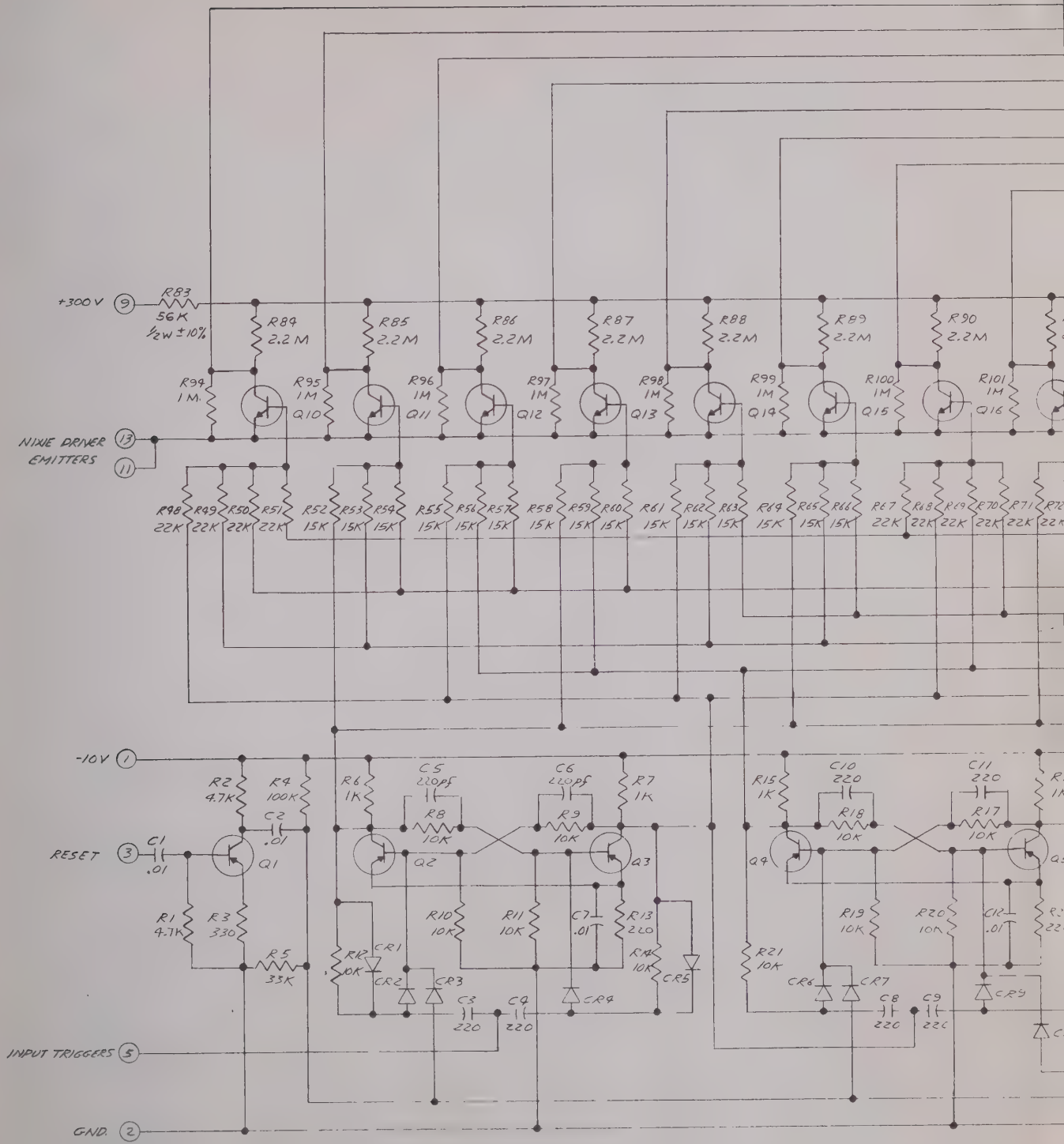
31 UNLESS OTHERWISE SPECIFIED

E-196.

REQ'D	ITEM	PART NO	DESCRIPTION	MATERIAL	SPEC.		WT	ZONE

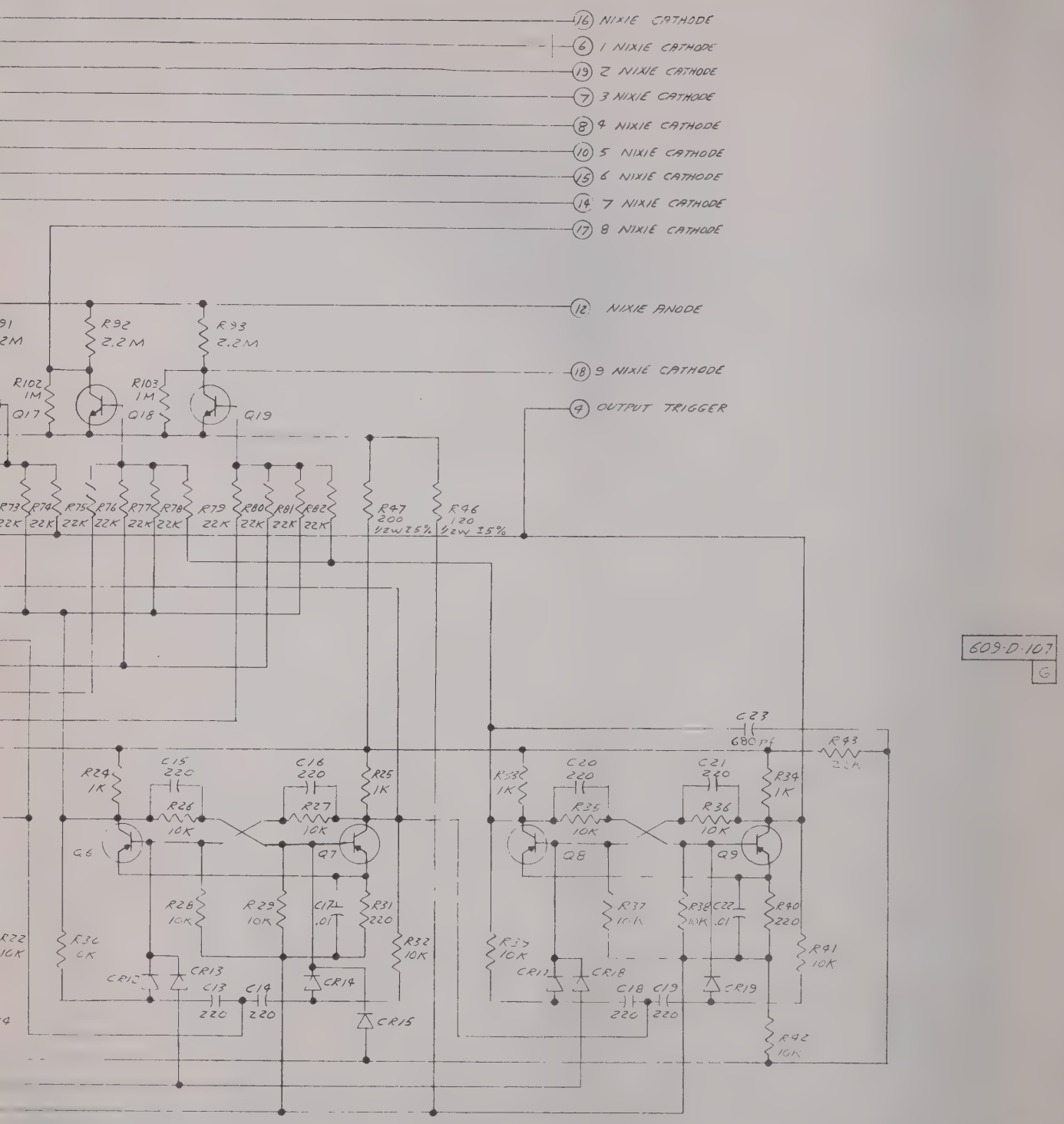
LIST OF MATERIALS

MATERIAL		TRANSISTOR SPECIALTIES, INC. PLAINVIEW, L.I., N.Y.	
HEAT TREAT		TITLE: SIGNAL DIVIDER	
FINISH			
BREAK ALL SHARP EDGES .010 R. MAX.	SCALE: 2/1		
TOLERANCES UNLESS SPECIFIED		DWN: DLL 6-24-64	DWG. NO. 609-D-195
FRACT.± ANGLES±		CKD.	
DEC..00± MACHINE FINISH		APP. RDB 7-2-64	SHT. OF REV.
DEC.000± RMS MU IN			
NEXT ASSY.	USED ON		



NOTES:

1. ALL DIODES ARE
2. TRANSISTORS Q1 TH
   AR' Q1CC2.
3. FOR PRINTED CKT



609-D-107
G

N191
Q3 ARE Q1001; Q10 THRU Q12
D. SEE DWG. 609-D-102

REQ'D	ITEM	PART NO	DESCRIPTION	MATERIAL	SPEC.		WT	ZONE

LIST OF MATERIALS

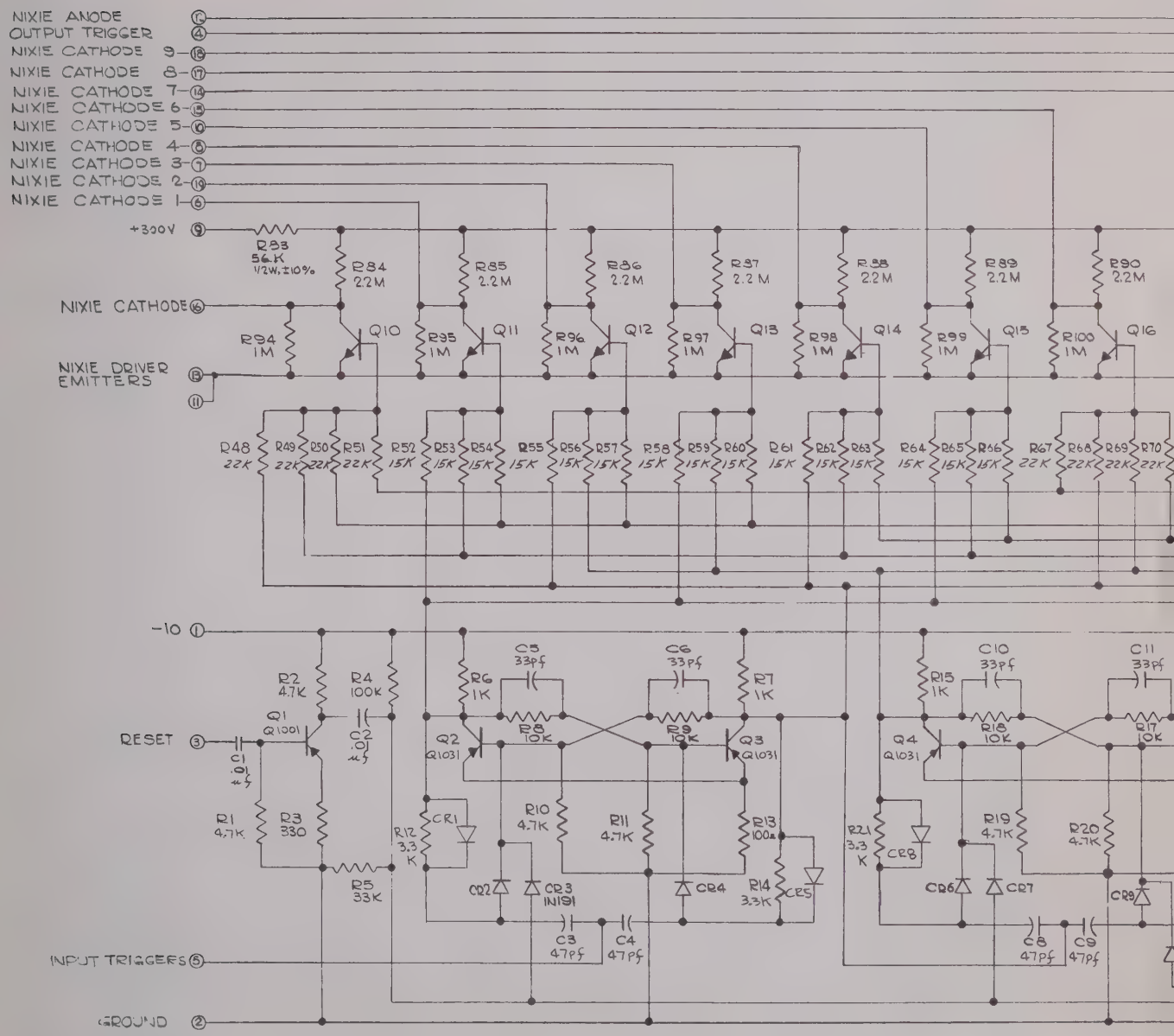
MATERIAL
HEAT TREAT
FINISH
BREAK ALL SHARP EDGES .010 R. MAX.
SCALE 2/1
TOLERANCES UNLESS SPECIFIED
FRACT ± ANGLES ±
DEC .00 ± MACHINE FINISH
DEC .000 ± RMS MU IN

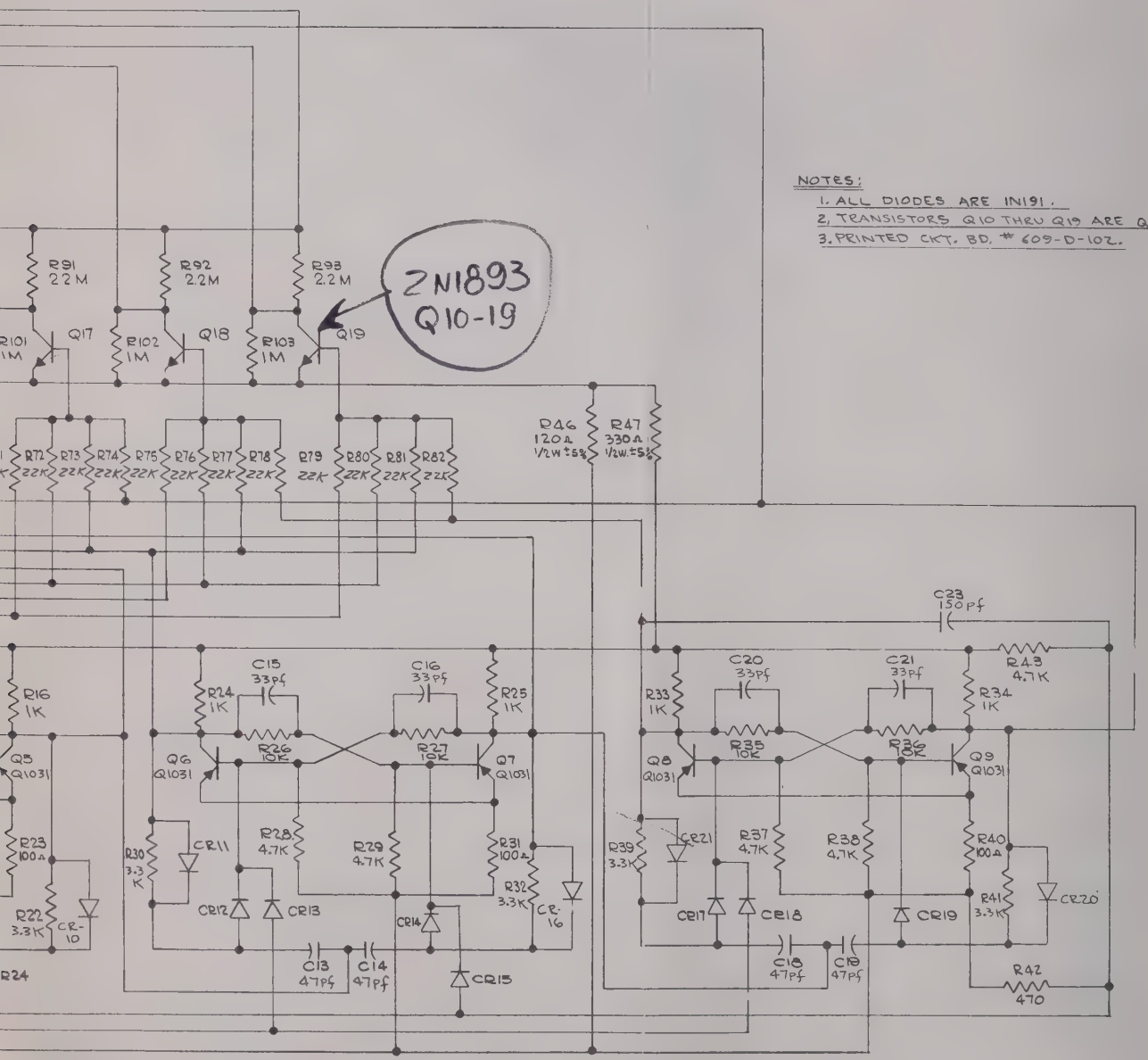
NEXT ASSY | USED ON

TRANSISTOR SPECIALTIES, INC.
PLAINVIEW, L.I., N.Y.

TITLE DECADE READOUT #22

DWN R.M. 9/6/65
CKD
APP
DWG NO 609-D-107
SHT OF REV

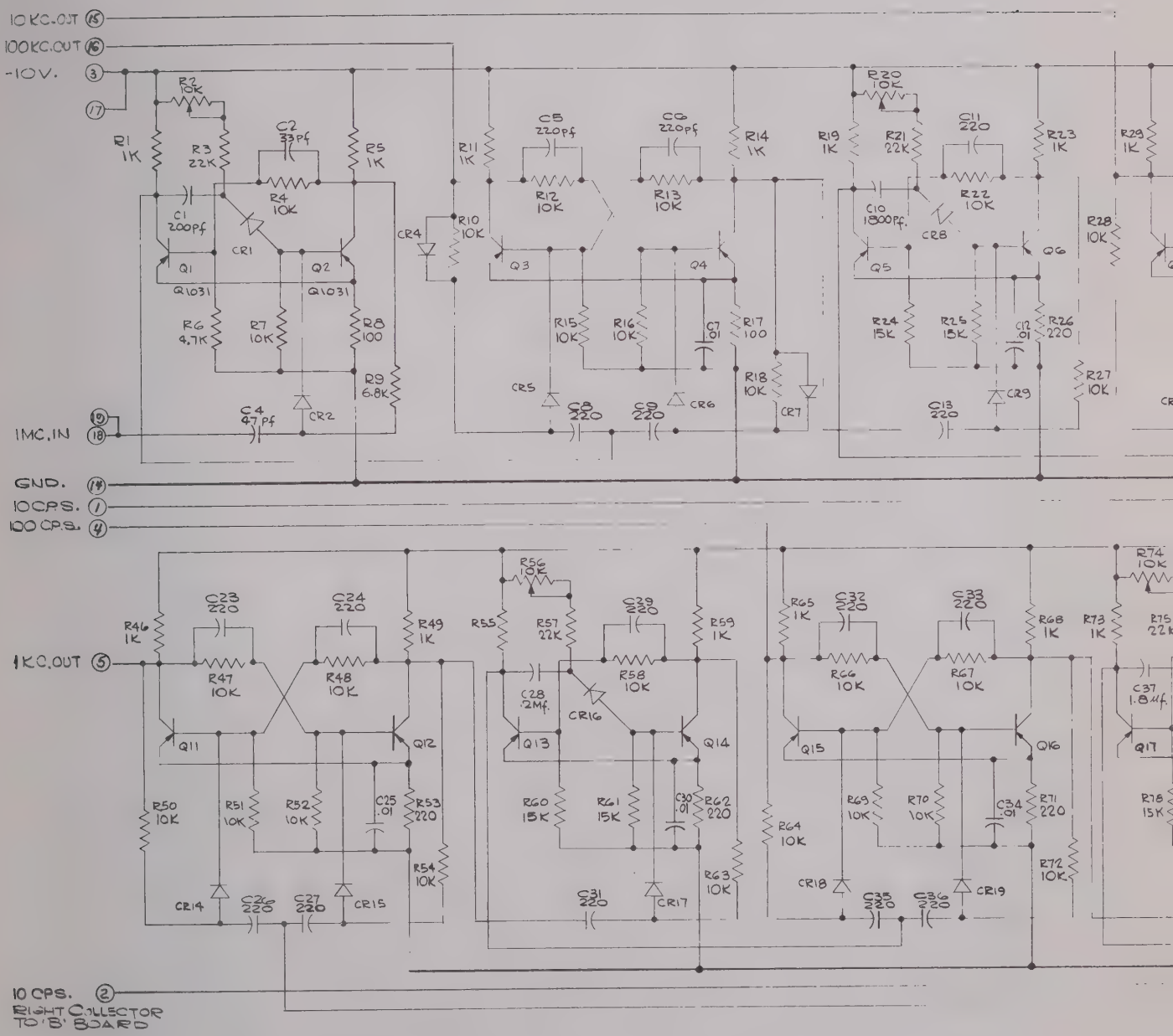

NIXIE ANODE 1
OUTPUT TRIGGER 4
NIXIE CATHODE 9 18
NIXIE CATHODE 8 17
NIXIE CATHODE 7 14
NIXIE CATHODE 6 15
NIXIE CATHODE 5 12
NIXIE CATHODE 4 8
NIXIE CATHODE 3 7
NIXIE CATHODE 2 19
NIXIE CATHODE 1 6
+300V 9
R83 56K 1/2W, ±10%
R84 2.2M
R85 2.2M
R86 2.2M
R87 2.2M
R88 2.2M
R89 2.2M
R90 2.2M
NIXIE CATHODE 16
R94 1M
Q10
R95 1M
Q11
R96 1M
Q12
R97 1M
Q13
R98 1M
Q14
R99 1M
Q15
R100 1M
Q16
NIXIE DRIVER EMITTERS 13 11
R48 22K
R49 22K
R50 22K
R51 22K
R52 15K
R53 15K
R54 15K
R55 15K
R56 15K
R57 15K
R58 15K
R59 15K
R60 15K
R61 15K
R62 15K
R63 15K
R64 15K
R65 15K
R66 15K
R67 22K
R68 22K
R69 22K
R70 22K
-10 1
R2 4.7K
R4 100K
C5 33pf
C6 33pf
R6 1K
R7 1K
C10 33pf
C11 33pf
R15 1K
Q1 Q1001
C2 .01 µf
R8 10K
R9 10K
R16 10K
R17 10K
RESET 3
C1 .01 µf
Q2 Q1031
Q3 Q1031
Q4 Q1031
R1 4.7K
R3 330
CR1
R10 4.7K
R11 4.7K
R13 100Ω
R21 3.3K
CR8
R19 4.7K
R20 4.7K
R12 3.3K
CR2
CR3 IN191
CR4
R14 3.3K
CR5
CR6
CR7
CR9
R5 33K
C3 47pf
C4 47pf
C8 47pf
C9 47pf
INPUT TRIGGERS 5
GROUND 2

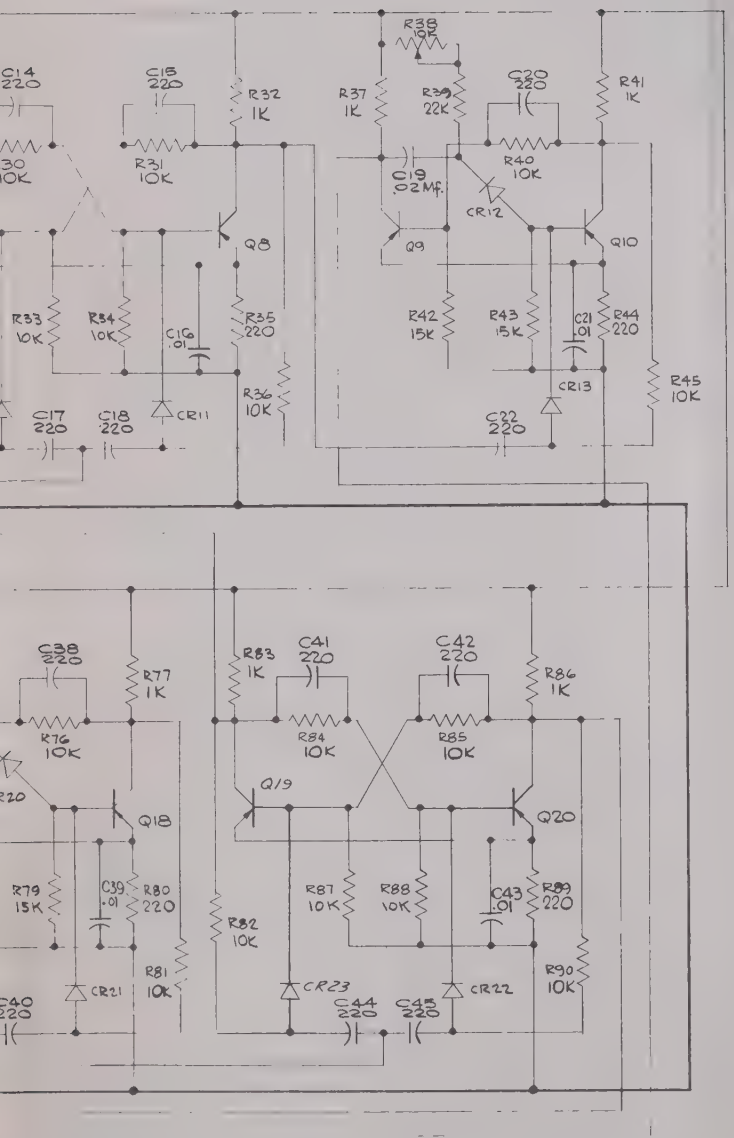


NOTES:

1. ALL DIODES ARE IN191.
2. TRANSISTORS Q10 THRU Q19 ARE Q1002.
3. PRINTED CKT. BD. # 609-D-102.

TITLE DECADE READOUT #21	ASSOCIATED DRAWINGS	
	DRAWN BY: M.F. DATE 5-5-60	
	CHKD BY. J.S. APPR. J.S. 5/7/60	609 D1106
TRANSISTOR SPECIALTIES INC.		REV. G

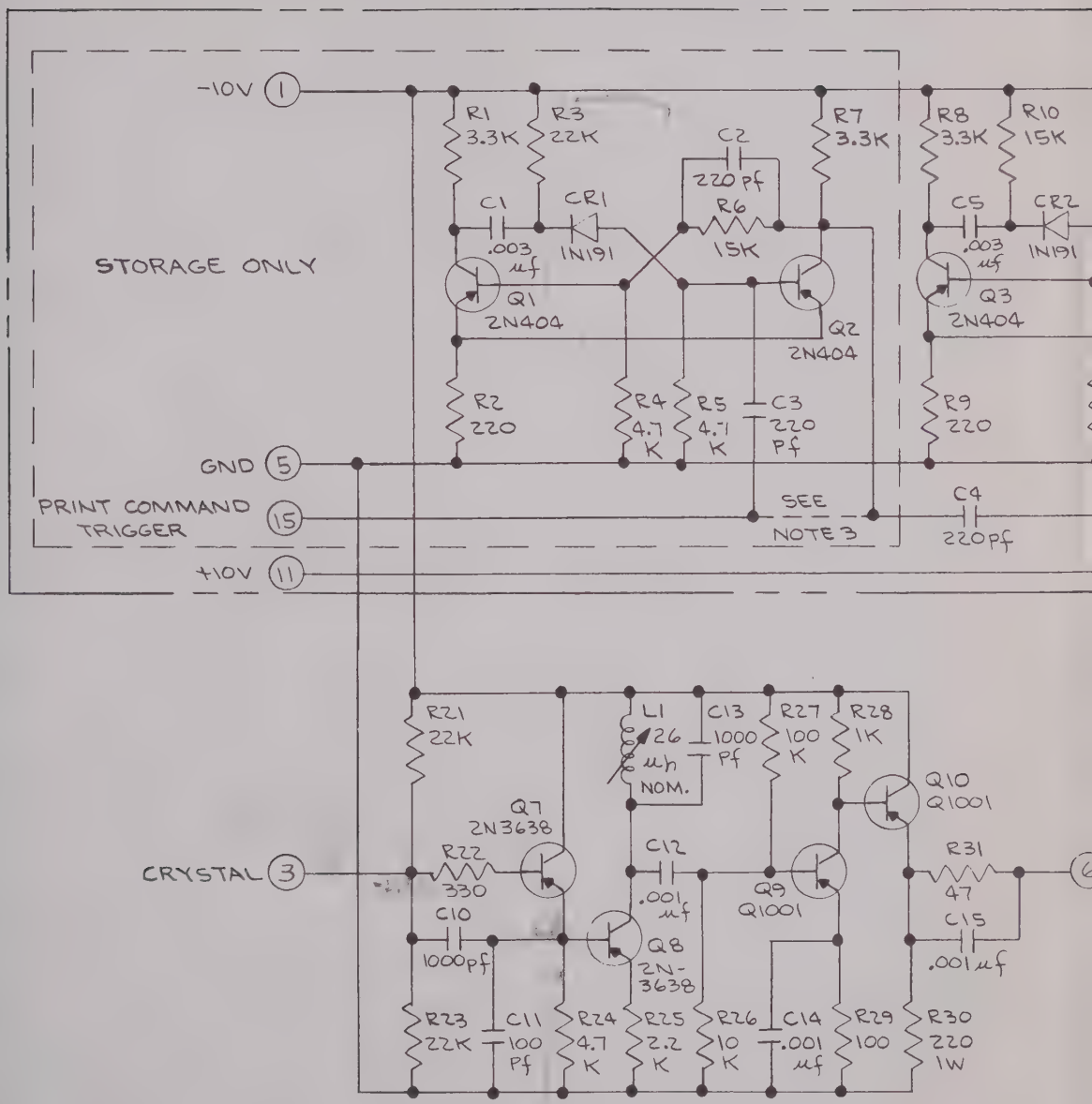

10 KC. OUT 15
100 KC. OUT 16
-10V. 3
17
R1 1K
R2 10K
R3 22K
C2 33pf
R4 10K
R5 1K
C1 200pf
CR1
Q1
Q2
Q1031
Q1031
R6 4.7K
R7 10K
R8 100
R9 6.8K
C4 47 pf
CR2
1MC. IN 19 18
GND. 14
10 CPS. 1
100 CPS. 4
R11 1K
C5 220pf
R12 10K
C6 220pf
R13 10K
R14 1K
R10 10K
CR4
Q3
Q4
R15 10K
R16 10K
C7 .01
R17 100
R18 10K
CR7
CR5
C8 220
C9 220
CR6
R19 1K
R20 10K
R21 22K
C11 220
R22 10K
R23 1K
C10 1800pf.
CR8
Q5
Q6
R24 15K
R25 15K
C12 .01
R26 220
R27 10K
CR9
C13 220
R28 10K
R29 1K
1 KC. OUT 5
R46 1K
C23 220
R47 10K
C24 220
R48 10K
R49 1K
Q11
Q12
R50 10K
R51 10K
R52 10K
C25 .01
R53 220
R54 10K
CR14
C26 220
C27 220
CR15
R55
R56 10K
R57 22K
C28 .2Mf.
CR16
C29 220
R58 10K
R59 1K
Q13
Q14
R60 15K
R61 15K
C30 .01
R62 220
R63 10K
C31 220
CR17
R64 10K
R65 1K
C32 220
RG6 10K
C33 220
R67 10K
R68 1K
Q15
Q16
R69 10K
R70 10K
C34 .01
R71 220
R72 10K
CR18
C35 220
C36 220
CR19
R73 1K
R74 10K
C37 1.8μf
Q17
R78 15K
10 CPS. 2
RIGHT COLLECTOR TO 'B' BOARD

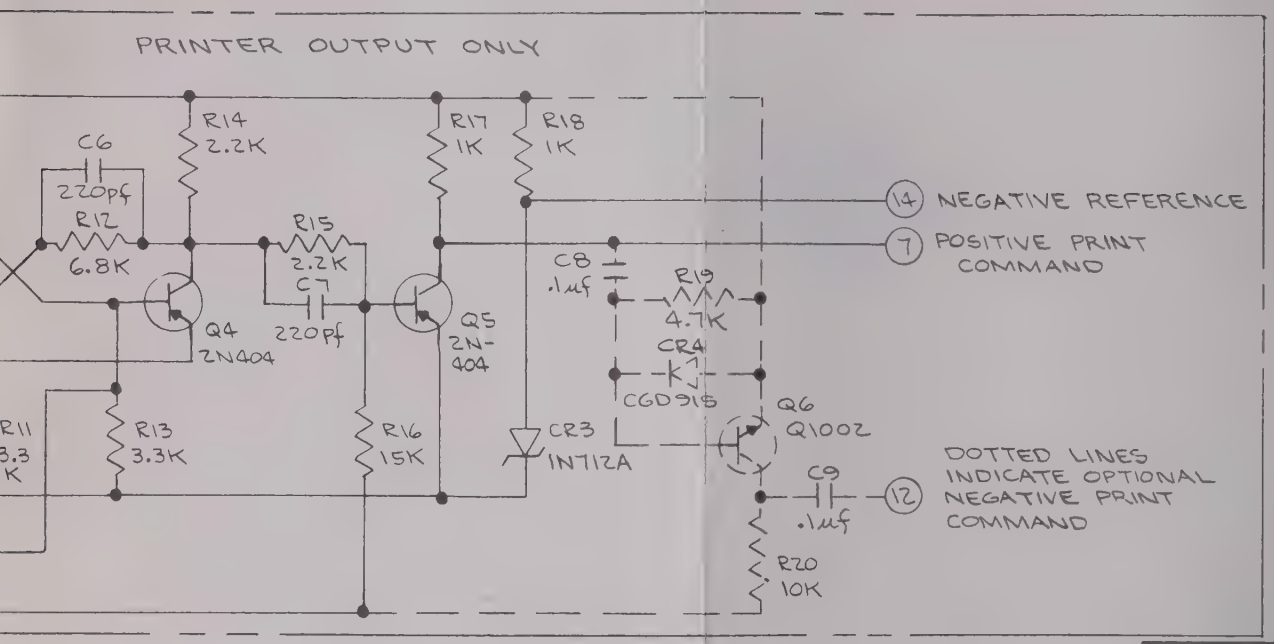


NOTES:

1. ALL DIODES ARE 1N191 UNLESS OTHERWISE SPECIFIED.
2. ALL TRANSISTOR ARE Q1001 (OR EQUIV.) UNLESS OTHERWISE SPECIFIED.

	↓ ASSOCIATED DRAWINGS ↓	
TITLE: TIME BASE GENERATOR	DRAWN SGL	DATE 5/17/60
	CHKD CJR	609|D|104
TRANSISTOR SPECIALTIES, INC	APPR [illegible]	REV. E


STORAGE ONLY
-10V 1
GND 5
PRINT COMMAND TRIGGER 15
+10V 11
R1 3.3K
R3 22K
C1 .003 µf
CR1 1N191
C2 220 pf
R6 15K
R7 3.3K
Q1 2N404
Q2 2N404
R2 220
R4 4.7 K
R5 4.7 K
C3 220 Pf
SEE NOTE 3
R8 3.3K
R10 15K
C5 .003 µf
CR2 1N191
Q3 2N404
R9 220
C4 220pf
CRYSTAL 3
R21 22K
L1 26 µh NOM.
C13 1000 Pf
R27 100 K
R28 1K
Q10 Q1001
Q7 2N3638
R22 330
C12 .001 µf
Q9 Q1001
R31 47
C10 1000pf
Q8 2N-3638
C15 .001 µf
R23 22K
C11 100 Pf
R24 4.7 K
R25 2.2 K
R26 10 K
C14 .001 µf
R29 100
R30 220 1W



609-C-215

A

IMC

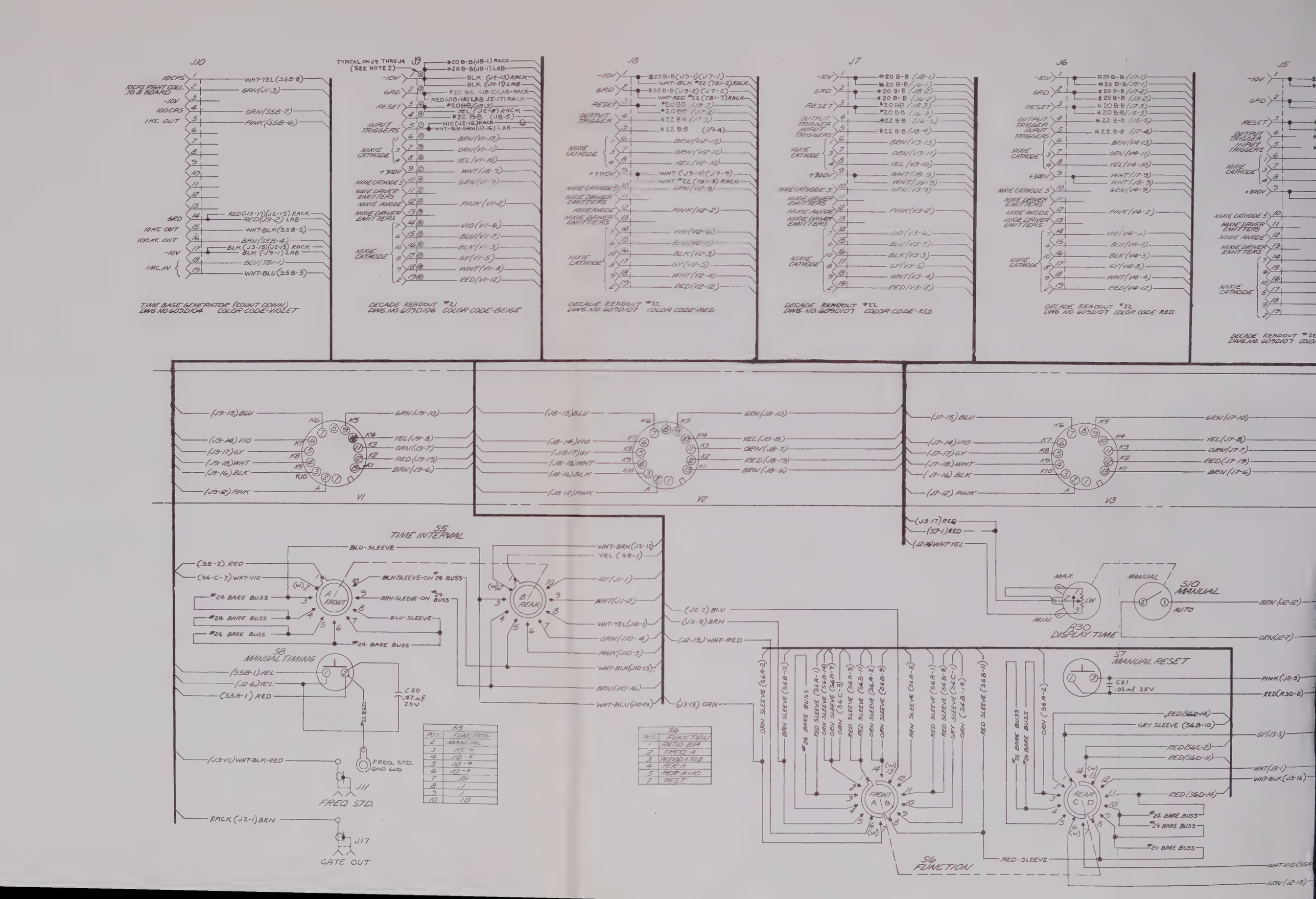
NOTES:

1. ALL RESISTORS ARE ½W UNLESS OTHERWISE SPECIFIED.
2. PRINTED CKT. BD. 609-D-210.
3. USE THIS CONNECTION WHEN USING PRINTER AND DELETING STORAGE.

REQ'D	ITEM	PART NO.	DESCRIPTION	MATERIAL	SPEC.		WT.	ZONE

LIST OF MATERIALS

		MATERIAL	TRANSISTOR SPECIALTIES, INC. PLAINVIEW, L.I., N.Y.
		HEAT TREAT	
		FINISH	TITLE: OSC. & PRINT COMMAND
		BREAK ALL SHARP EDGES .010 R MAX. SCALE ~	
		TOLERANCES UNLESS SPECIFIED	DWN. 10-8-65 DWG.NO 609-C-215
		FRACT.= ANGLES=	CKD.
		DEC.00= MACHINE FINISH	APP. SHT. OF REV A
NEXT ASSY.	USED ON	DEC.000= RMS MU IN	


J10
TIME BASE GENERATOR (COUNT DOWN)
DWG NO 609D106A COLOR CODE-VIOLET
J9
TYPICAL ON J9 THRU J4 (SEE NOTE 2)
DECADE READOUT #21
DWG. NO. 609D106 COLOR CODE-BEIGE
J8
DECADE READOUT #22
DWG. NO. 609D107 COLOR CODE-RED
J7
DECADE READOUT #22
DWG. NO. 609D107 COLOR CODE-RED
J6
DECADE READOUT #22
DWG. NO. 609D107 COLOR CODE-RED
J5
V1
V2
V3
S5 TIME INTERVAL
S8 MANUAL TIMING
FREQ STD.
GATE OUT
S7 MANUAL RESET
S6 FUNCTION
R30 DISPLAY TIME
S10 MANUAL
FRONT A B
REAR C D

A	195 PER ECO #200	KW	2-7-64	
B	AS PER ECO #261	KW	2-8-64	
C	AS PER ECO #262	KW	2-10-64	
D	AS PER ECO #272	KW	2-17-64	
E	AS PER ECO #328	KW	3-17-64	
F	AS PER ECO #339	KW	3-11-64	
G	AS PER ECO #554	KW	7-1-64	
H	AS PER ECO #557	KW	7-15-64	
I	AS PER ECO #756	KW	9-23-64	
K	AS PER ECO #802	KW	10-13-64	
L	AS PER ECO #866	KW	10-27-64	
M	AS PER ECO #865	KW	10-27-64	
N	AS PER ECO #912	TR	11-24-64	
P	AS PER ECO #986	KW	01-7-65	

J4

-10V
GRD
RESET
INPUT TRIGGERS
NIXIE CATHODES
NIXIE DRIVER EMITTERS
+300V
NIXIE CATHODES
NIXIE DRIVER EMITTERS
NIXIE ANODE
NIXIE DRIVER EMITTERS
NIXIE CATHODE

BLK (TB1-2) LAB
BLK (J5-1) (J3-15) LAB
#20 B-B (J5-1) RACK
RED (TB1-9) LAB
RED (J6-2) (J3-17) LAB
#20 B-B (J5-2) RACK
#20 B-B (J5-3) LAB & RACK
YEL (J2-8) LAB
#22 B-B (J5-4)
BRN (V6-13)
ORN (V6-11)
YEL (V6-10)
WHT (TB1-7) LAB
WHT (J5-9)
GRN (V6-9)
PINK (V6-2)
VIO (V6-6)
BLU (V6-7)
BLK (V6-3)
GY (V6-5)
WHT (V6-4)
RED (V6-12)

DECADE READOUT #22
DWG NO. 609D107 COLOR CODE - RED

J3

"A" TRIGGERS
"A" SCHMITT
"B" TRIGGERS
"B" SCHMITT
A×10 OUT
FREQ STD
TIME BASE TRIGGERS
TIME BASE
-10V
A×10 TRIGGERS
GRD

WHT (S6D-13)
PINK (S3-6)
GY (S6C-1)
BLU (S4-6)
BRN (S6A-5)
WHT-BLK-RED (J11)
WHT-BRN (S5B-2)
ORN (S6A-7)
BLK (J10-17) (J1-13) RACK
BLK (J9-1) (J2-15) LAB
WHT-BLK (S6D-12)
RED (J10-19) (J1-18) RACK
RED (J9-2) (J2-17) LAB
RED (R30-1 & 2)

SIGNAL DIVIDER
DWG NO. 609D195 COLOR CODE - WHITE

J2

GATE OUT
GATE RESET IN
PRINTER READOUT ONLY
MANUAL RESET IN
MANUAL TIME BASE IN
MANUAL SW
RESET OUT
GRD
MANUAL SW
DISPLAY TIME LOW END
-10V
COUNTER TRIGGERS
GRD
COUNTER IN
GATE TRIGGER IN

BRN (J17) RACK
BRN (TB1-6) LAB
BLU (S6B-13)
(SEE NOTE 5) VIO - (J16-15) LAB
VIO - (TB1-11) RACK
PINK (S7-2)
YEL (S8-1)
ORN (S10-2)
YEL (J9-3) RACK
YEL (J9-3) LAB
BRN (S10-1)
WHT-YEL (R30-3)
BLK (J3-15) (J1-19) LAB
BLK (J10-17) (J9-1) RACK
WHT-BLK-GRN (J9-5) LAB
MIC (J9-5) RACK
RED (J10-18) (J3-2) RACK
RED (J3-17) (J1-18) LAB
GRN (S6C-6)
WHT-RED (S6A-6)

GATING LOGIC
DWG NO. 609D194 COLOR CODE - YELLOW

J1

VIO CRS OUT
ICPS OUT
10 CPS IN
"C" TRIG POT HI END
"B" TRIG POT LOW END
OUT "B" SCHMITT
ONES OUT
ZEROS OUT
GRD
"B" INPUT
-7.5V IN
"A" INPUT
GRD
OUT "A" SCHMITT
ZEROS OUT
ONES OUT
"A" TRIG POT LOW END
"A" TRIG POT CENTER ARM
GRD
-10V

GY (S5B-10)
WHT (S5B-9)
GRN (J10-2)
WHT-GRN (R48)
WHT-BRN (R48)
YEL (S4-2)
VIO (S4-1)
RED
RED (TB1-5) RACK
RED
(A1-1)
RED (J11-13)
BLK (TB1-9) RACK
MIKE WIRE (TB1-8) LAB
WHT-BLK-ORN (S3-BLANK PIN OR TIE POINT)
(A1-2)
RED
RED (SHLD OF J1-9)
ORN (S3-1)
BRN (S3-2)
WHT-YEL (R45-3)
WHT-VIO (R45-1)
RED (CHASSIS GND)
RED (J3-17) RACK
RED (J2-17) LAB
BLK (J3-15) RACK
BLK (J2-15) LAB

INPUT AMPLIFIER
DWG NO. 609D103 COLOR CODE - BLUE

TB1

(J10-18) BLU - IMC
(J9-1) BLK - -10V
(DS1-1) BLK - PILOT LAMP
(S2-1) RED - POWER SW.
(S2-2) WHT - POWER SW.
(J2-1) BRN - GATE OUT
(J9-9) WHT - +300V
(J1-10) MIKE WIRE - -7.5V
(J8-2) RED - GND
RED
RED

FOR OTHER HALF OF TB1 SEE POWER SUPPLY WIRING DIA. DWG. NO. 609-D-157

TERMINAL BOARD FOR 361 LAB

TB1

(J10-18) BLU - IMC
(J8-1) #22 WHT-BLK - -10V
(J8-9) #22 WHT - +300V
(J1-10) BLK - -7.5V
(J1-8) RED
RED
(J8-2) #22 WHT-RED - GND
RED
(S2-1) RED - POWER SW.
(S2-2) WHT - POWER SW.
(DS1-1) BLK - PILOT LAMP
(J2-9) VIO - THIS WIRE IS ON ALL RACK MODELS WITH PRINTER READOUT; ON RACKS WITHOUT PRINTER READOUT THIS WIRE IS TIED BACK IN HARNESS.

11 THRU 15 USED ONLY W/ PRINTER READOUT MODEL

TERMINAL BOARD FOR 361 RACK

WIRING DIA. AT THIS POINT BECOMES AS FOLLOWS:
A. TO POWER SUPPLY ON 361 LAB AS SHOWN.
B. TO POWER SUPPLY ON 361 RACK AS SHOWN.
C. FOR WIRING OF PRINTER READOUT CONNECTOR SEE DWG. 620-C-155.

(J6-15) BLU
(J6-14) VIO
(J6-17) GY
(J6-18) WHT
(J6-16) BLK
(J6-12) PINK
K6 K5 K7 K8 K9 K10 K4 K3 K2 K1 A
GRN (J6-10)
YEL (J6-8)
ORN (J6-7)
RED (J6-19)
BRN (J6-6)

V4

(J5-15) BLU
(J5-14) VIO
(J5-17) GY
(J5-18) WHT
(J5-16) BLK
(J5-12) PINK
K6 K5 K7 K8 K9 K10 K4 K3 K2 K1 A
GRN (J5-10)
YEL (J5-8)
ORN (J5-7)
RED (J5-19)
BRN (J5-6)

V5

(J4-15) BLU
(J4-14) VIO
(J4-17) GY
(J4-18) WHT
(J4-16) BLK
(J4-12) PINK
K6 K5 K7 K8 K9 K10 K4 K3 K2 K1 A
GRN (J4-10)
YEL (J4-8)
ORN (J4-7)
RED (J4-19)
BRN (J4-6)

V6

YEL (J1-6)
VIO (J1-7)
BLU (J3-6)
WHT-BLK-ORN (S3 TIE POINT)
(+) (-) 6 2
(TIE POINT) #6035 LERCO TERMINAL

ALTERNATE S4 INPUT "B" TRIGGER SLOPE

(S4 TIE POINT) WHT-BLK-ORN
(J1-10) WHT-BLK-ORN
(J3-2) PINK
(J1-14) ORN
(J1-15) BRN
(TIE POINT) #6035 LERCO TERMINAL

ALTERNATE S3 INPUT "A" TRIGGER SLOPE

WHT-BLK-ORN
BLK-WHT-ORN (S3-4)
YEL (J1-6)
VIO (J1-7)
(+) (-) 2 3 4 5 6 (W) 12 11 10 9 8 7
S4 INPUT "B" TRIGGER SLOPE
BLU (J3-6)
R47 4.7K
WHT-GRN (J1-4)
WHT-BRN (J1-5)
CW
R48 INPUT "B" TRIGGER LEVEL

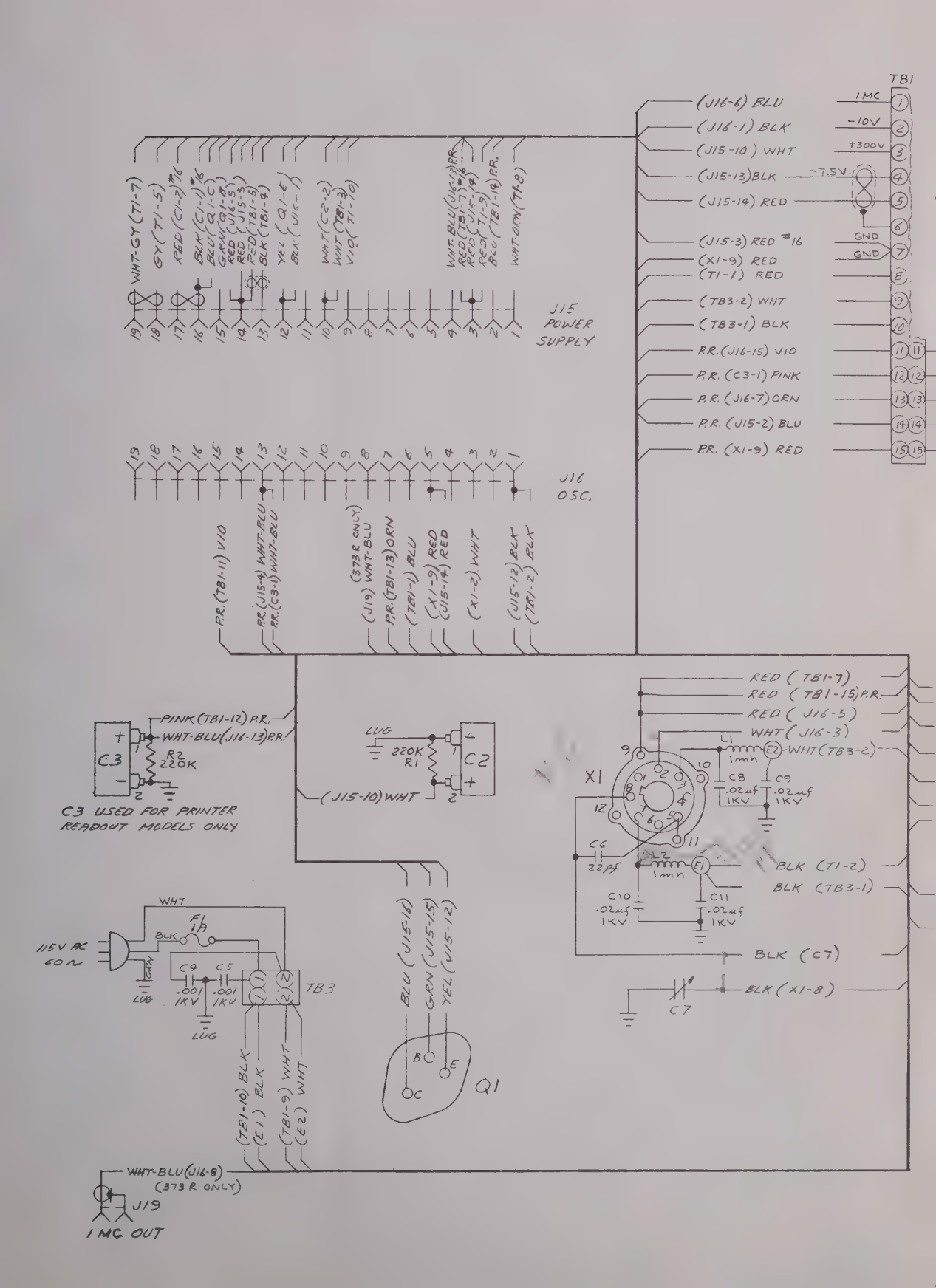
WHT-BLK-ORN
(J1-14) ORN
(J1-15) BRN
(J1-10) WHT-BLK-ORN
(S4-4) WHT-BLK-ORN
(J3-2) PINK
S3 INPUT "A" TRIGGER SLOPE
R46 4.7K
WHT-VIO (J1-17)
WHT-YEL (J1-16)
CW
R45 INPUT "A" TRIGGER LEVEL

(J1-9)
(J1-12)
ATTENUATOR ASSEMBLY A1
"B"
"A"
1 2
J13 INPUT
J12 INPUT

BLK (TB1-3) LAB
BLK (TB1-10) RACK
DS1 POWER ON
R40 18K
RED (TB1-4) LAB
RED (TB1-8) RACK
WHT (TB1-5) LAB
WHT (TB1-9) RACK
TO CHASSIS GND AT ATTENUATOR SHIELD
OFF ON
S2 POWER ON-OFF

NOTES:
1. ALL VALUES EXPRESSED IN OHMS AND MICROMICROFARADS. K DENOTES 1000 OHMS.
2. NUMBERS ENCLOSED IN CIRCLES, ON CONNECTORS J4 THRU J9 ONLY, REFER TO WIRING CONNECTIONS ON UNITS WITH SERIAL NUMBERS 272 THRU 314.
3. THIS DWG USED FOR BOTH MODELS 361 & 361R IMC APPT-METER
4. PRINTER READOUT CONNECTOR IS OPTIONAL FOR BOTH 361 & 361-R
5. FOR 361 LAB WITH PRINTER READOUT ONLY
6. B-B DENOTES BARE BUSS.

MOD. 361 AND 361-R	← ASSOCIATED DRAWINGS →	
TITLE INTERCONNECTION SCH. & WIRING DIAG	DRAWN BY KW	DATE 8-25-60
	CHKD. F. [illegible]	609E144
	APPD. F. [illegible]	
TRANSISTOR SPECIALTIES, INC.		REV P

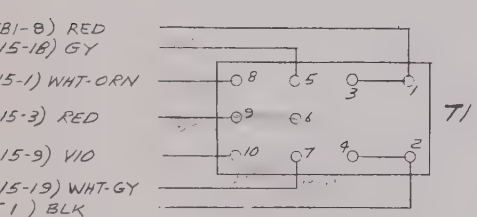

TB1
1MC
-10V
+300V
-7.5V
GND
GND
(J16-6) BLU
(J16-1) BLK
(J15-10) WHT
(J15-13) BLK
(J15-14) RED
(J15-3) RED #16
(X1-9) RED
(T1-1) RED
(TB3-2) WHT
(TB3-1) BLK
P.R. (J16-15) VIO
P.R. (C3-1) PINK
P.R. (J16-7) ORN
P.R. (J15-2) BLU
P.R. (X1-9) RED
WHT-GY (T1-7)
GY (T1-5)
RED (C1-2) #16
BLK (C1-1) #16
BLU (Q1-C)
GRN (Q1-B)
RED (J16-5)
RED (J15-3)
RED (TB1-3)
BLK (TB1-4)
YEL (Q1-E)
BRN (J16-1)
WHT (C2-2)
WHT (TB1-3)
VIO (T1-10)
WHT-BLU (J16-13) P.R.
RED (TB1-7) #16
RED (J15-3) #16
RED (T1-9) P.R.
BLU (TB1-14) P.R.
WHT-ORN (T1-8)
J15 POWER SUPPLY
J16 OSC.
P.R. (TB1-11) VIO
P.R. (J15-4) WHT-BLU
P.R. (C3-1) WHT-BLU
(J19) WHT-BLU (373 R ONLY)
P.R. (TB1-13) ORN
(TB1-1) BLU
(X1-9) RED
(J15-14) RED
(X1-2) WHT
(J15-12) BLK
(TB1-2) BLK
PINK (TB1-12) P.R.
WHT-BLU (J16-13) P.R.
C3
R2 220K
C3 USED FOR PRINTER READOUT MODELS ONLY
LUG
220K R1
C2
(J15-10) WHT
RED (TB1-7)
RED (TB1-15) P.R.
RED (J16-5)
WHT (J16-3)
WHT (TB3-2)
X1
L1 1mh
E2
C8 .02uf 1KV
C9 .02uf 1KV
C6 22pf
L2 1mh
E1
C10 .02uf 1KV
C11 .02uf 1KV
BLK (T1-2)
BLK (TB3-1)
BLK (C7)
BLK (X1-8)
C7
WHT
115V AC 60~
BLK
GRN
F1 1A
LUG
C4 .001 1KV
C5 .001 1KV
TB3
LUG
(TB1-10) BLK
(E1) BLK
(TB1-9) WHT
(E2) WHT
BLU (J15-16)
GRN (J15-15)
YEL (J15-12)
B
E
C
Q1
WHT-BLU (J16-8) (373 R ONLY)
J19
1MC OUT

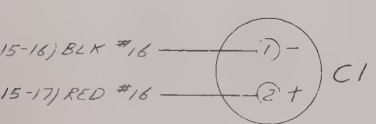
2 OTHER HALF OF TB1 SEE WIRING DIA. FOR :
373 LAB & RACK DWG. 631-E-05
371 LAB & RACK DWG. 630-E-03
361 LAB & RACK DWG. 609-E-194

V10 (J2-9) P.R. DWG NO 631-E-05
PINK (J19-3) P.R.
ORN (J19-79) P.R.
BLU (J19-78) P.R.
RED (J19-82) P.R.

11 THRU 15 USED ONLY ON PRINTER READOUT MODELS

12 THRU 15 GO TO J19 (PRINTER READOUT CONNECTOR) DWG. 620-C-155



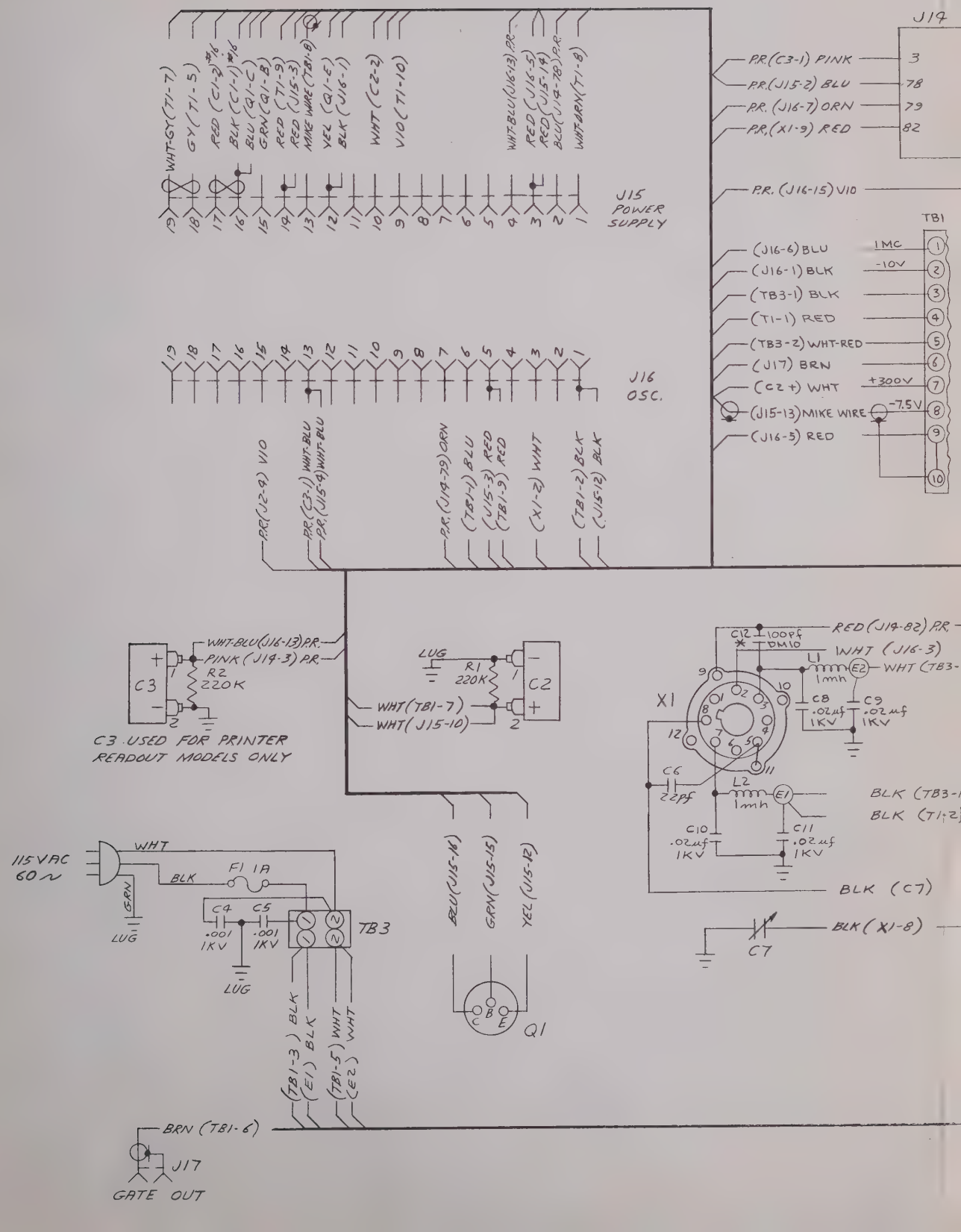


NOTES :
1. P.R. MEANS PRINTER READOUT
2. PRINTER READOUT CONNECTOR IS OPTIONAL

REQ'D	ITEM	PART NO	DESCRIPTION	MATERIAL	SPEC.		WT.	ZONE

LIST OF MATERIALS

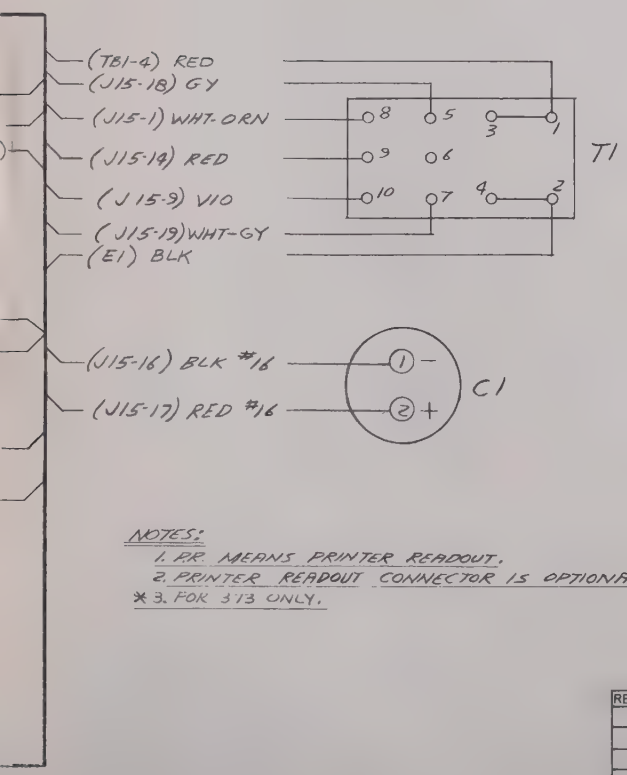
		MATERIAL	TRANSISTOR SPECIALTIES, INC. PLAINVIEW, L.I., N.Y.		
		HEAT TREAT			
		FINISH	TITLE POWER SUPPLY WIRING DIAGRAM RACK (SEE NEXT ASS'Y)		
631-E-05	373 & 373-R	BREAK ALL SHARP EDGES .010 R. MAX. SCALE N			
630-E-03	371 & 371-R	TOLERANCES UNLESS SPECIFIED	DWN RW	7-29-11	DWG. NO. 620-D-154
609-E-194	361 & 361-R	FRACT ± ANGLES ±	CKD.		
		DEC. .00 ± MACHINE FINISH	APP.		
NEXT ASSY.	USED ON	DEC. .000 ± RMS MU IN		8-4-62	SHT. OF REV. D


J17
P.R.(C3-1) PINK
P.R.(J15-2) BLU
P.R. (J16-7) ORN
P.R.(X1-9) RED
3
78
79
82
P.R. (J16-15) V10
TB1
(J16-6) BLU
(J16-1) BLK
(TB3-1) BLK
(T1-1) RED
(TB3-2) WHT-RED
(J17) BRN
(C2+) WHT
(J15-13) MIKE WIRE
(J16-5) RED
1MC
-10V
+300V
-7.5V
J15 POWER SUPPLY
J16 OSC.
WHT-GY(T1-7)
GY(T1-5)
RED (C1-2) #16
BLK (C1-1) #16
BLU (Q1-C)
GRN (Q1-B)
RED (T1-3)
RED (J15-3)
NIKE WIRE (TB1-8)
YEL (Q1-E)
BLK (J16-1)
WHT (C2-2)
V10 (T1-10)
WHT-BLU(J16-13) P.R.
RED (J16-5)
RED(J15-14)
BLU(J14-28) P.R.
WHT-BRN(T1-8)
P.R.(J2-9) V10
P.R.(C3-1) WHT-BLU
P.R.(J15-9) WHT-BLU
P.R.(J14-29) ORN
(TB1-1) BLU
(J15-3) RED
(TB1-3) RED
(X1-2) WHT
(TB1-2) BLK
(J15-12) BLK
C3
R2 220K
WHT-BLU(J16-13) P.R.
PINK (J19-3) P.R.
C3 USED FOR PRINTER READOUT MODELS ONLY
LUG
R1 220K
C2
WHT(TB1-7)
WHT(J15-10)
C12 100pf DM10
RED (J19-82) P.R.
WHT (J16-3)
L1 1mh
WHT (TB3-
X1
C8 .02mf 1KV
C9 .02mf 1KV
C6 22pf
L2 1mh
BLK (TB3-
BLK (T1-2)
C10 .02mf 1KV
C11 .02mf 1KV
BLK (C7)
BLK (X1-8)
C7
115VAC 60~
WHT
BLK
GRN
LUG
F1 1A
C4 .001 1KV
C5 .001 1KV
LUG
TB3
BLU(J15-14)
GRN(J15-15)
YEL (J15-12)
Q1
(TB1-3) BLK
(E1) BLK
(TB1-5) WHT
(E2) WHT
BRN (TB1-6)
J17
GATE OUT

PRINTER READOUT CONNECTOR
(SEE DWG. #620-C-155 FOR
COMPLETE CONNECTOR)

TO (J2-9) V10 - ON DWG: 631-E-05 - 373 LAB & RACK
(THIS WIRE USED FOR PRINTER READOUT MODELS ONLY) 630-E-03-371 LAB & RACK
609-E-144-361 LAB & RACK

FOR OTHER HALF OF TB1 SEE WIRING DIA. FOR:
373 LAB & RACK DWG. 631-E-05
371 LAB & RACK DWG. 630-E-03
361 LAB & RACK DWG. 609-E-144

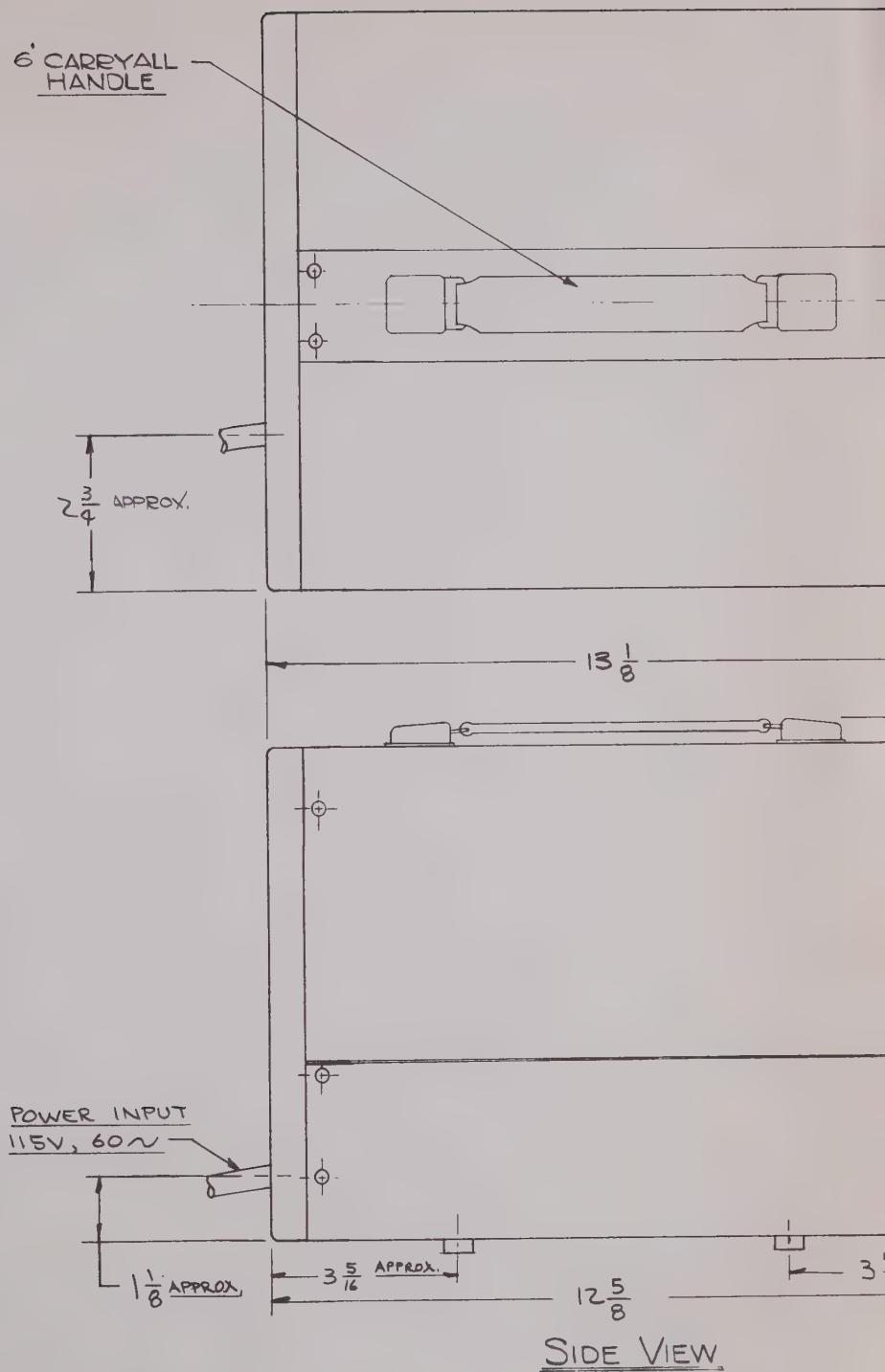


NOTES:
1. RR MEANS PRINTER READOUT.
2. PRINTER READOUT CONNECTOR IS OPTIONAL.
* 3. FOR 373 ONLY.

REQ'D	ITEM	PART NO	DESCRIPTION	MATERIAL	SPEC.		WT.	ZONE

LIST OF MATERIALS

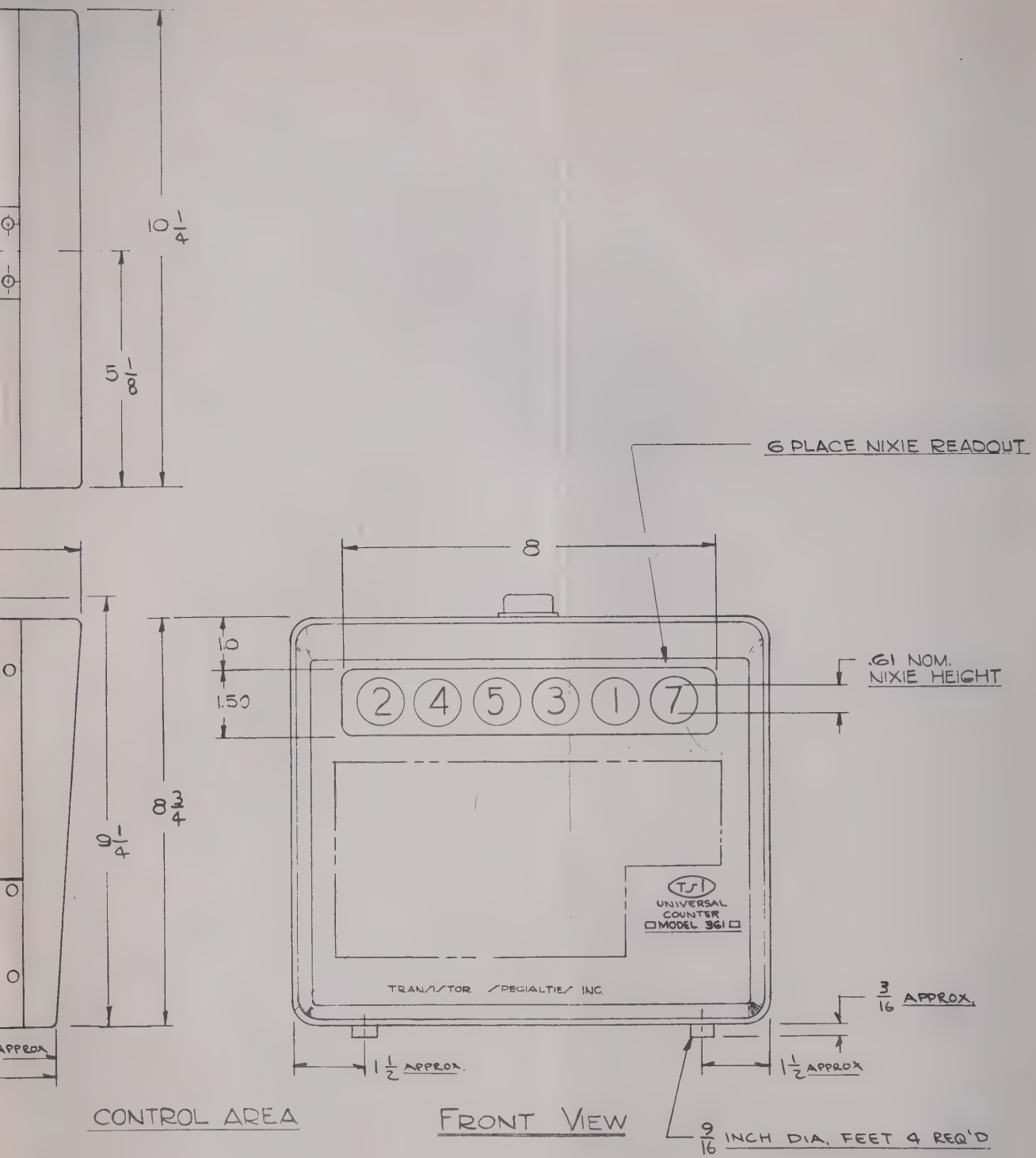
		MATERIAL	TRANSISTOR SPECIALTIES, INC. PLAINVIEW, L.I., N.Y.
		HEAT TREAT	
		FINISH	TITLE POWER SUPPLY WIRING DIA. LAB. (SEE NEXT ASS'Y)
		BREAK ALL SHARP EDGES .010 R. MAX. SCALE 2	
631-E-05	373 & 373-R	TOLERANCES UNLESS SPECIFIED	DWN. RW 5-22-61 DWG. NO. 609-D-157
630-E-03	371 & 371-R	FRACT ± ANGLES ±	CKD.
609-E-144	361 & 361-R	DEC.00 ± MACHINE FINISH	APP. SDR 10-2-62 SHT. OF REV. E
NEXT ASSY	USED ON	DEC.000 ± RMS MU IN	



SIDE VIEW

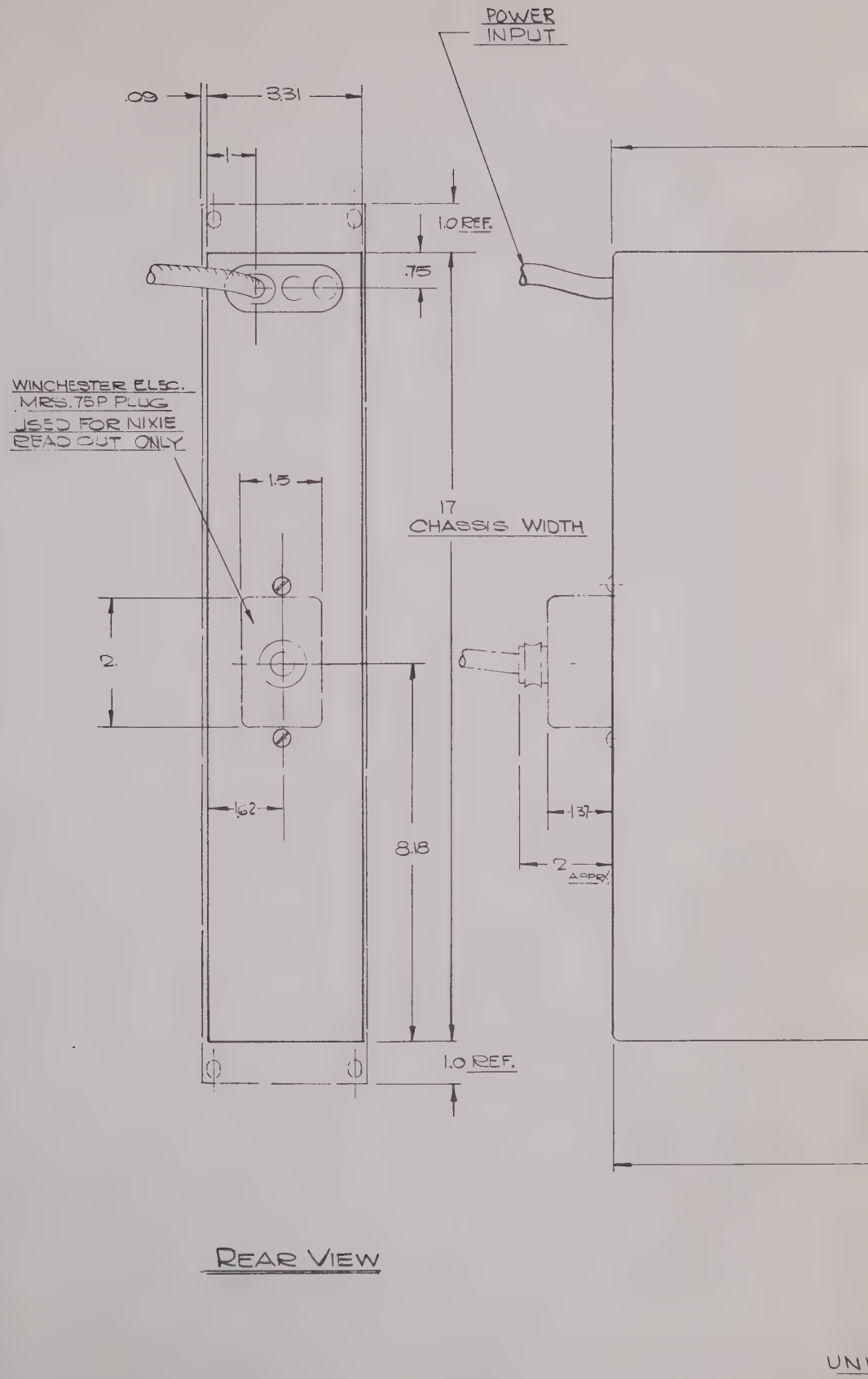
UNIVER

CABINE



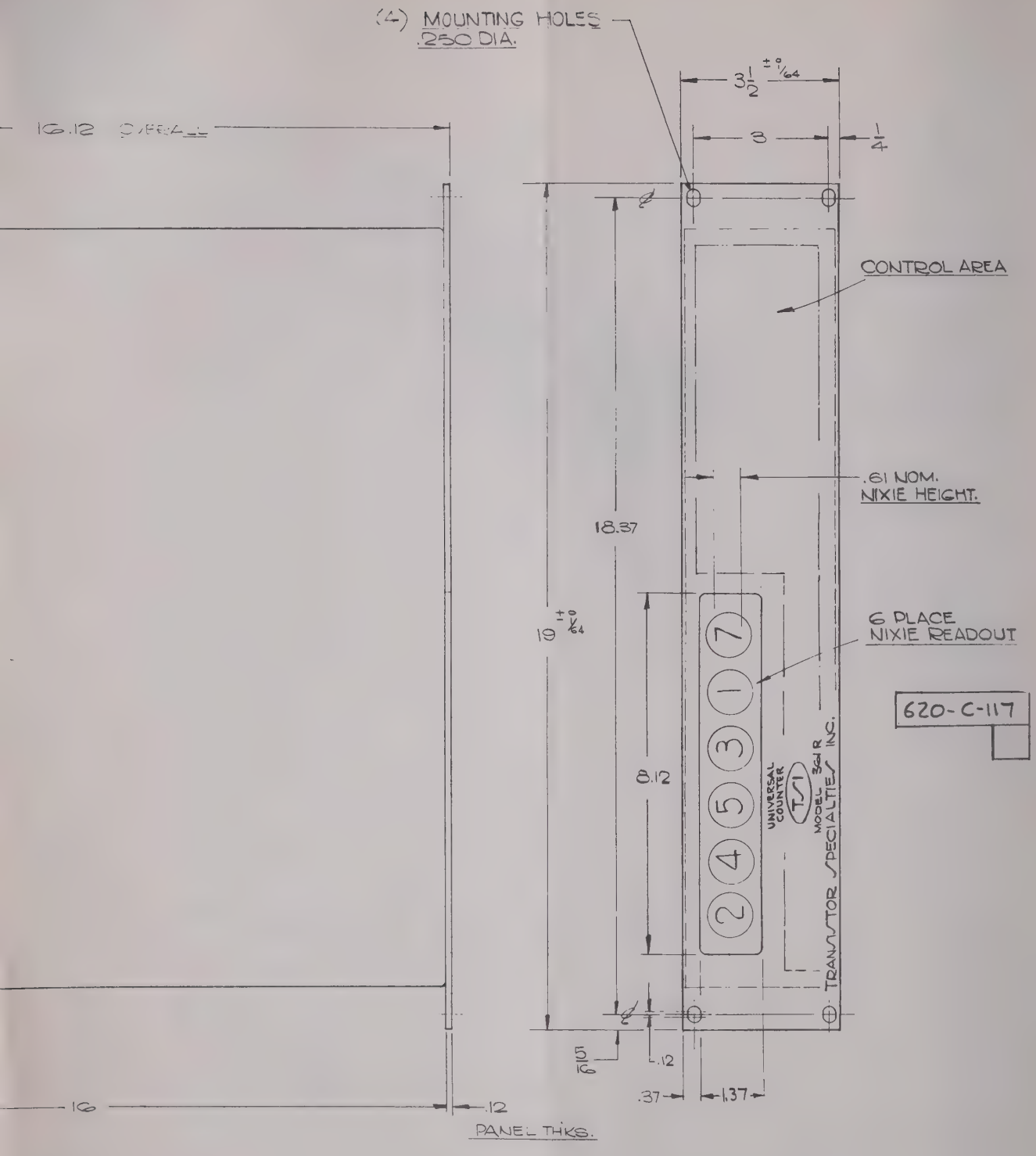
SAL COUNTER
T MODEL 361

TITLE: UNIVERSAL COUNTER, MODEL 361 OUTLINE DIMENSIONS	DRAWN BY MJ	DATE 11-16-60
	CHECKED BY	609-C-131
	APPROVED BY RTS	
TRANSISTOR SPECIALTIES INC.	SCALE-HALF.	REV. C



REAR VIEW

UNI
RACK



TOP VIEW

FRONT VIEW

ERSAL COUNTER
OUNT MODEL 361R

TITLE GEN. OUTLINE DIMENSIONS RACK MOUNT, 361R	DRAWN BY CHK'D BY APPV'D BY. SDR	DATE. 11-15-60 620-C-117
TRANSISTOR SPECIALTIES INC.	SCALE. HALF	REV.

SECTION VIII

PARTS LIST

GENERAL

The following list of parts is included to permit enigneering repairs to the Counter if necessary. Part numbers refer to the schematic diagrams included in Section VII of this manual.

The list of parts has been broken down by assemblies; either printed boards, major or sub-chassis, and the parts associated with each are indicated under the schematic drawing number preceding the particular list. The conventional symbols are used: Q for transistor, C for capacitor, R for resistor etc. The printed boards themselves are designated TB; for example TB 2001. Where the designation "Q1 to Q9" appears, it indicates identical components-in this case transistors.

Please note that some seemingly standard components actually are selected at manufacture for specific characteristics. As a result, parts replacement, particualarly on printed boards, should be followed by complete testing as per Section VII. It is recommended that printed boards be replaced as units and the defective board returned to the factory for repair. Inquiries concerning this should be addressed to:

Transistor Specialties, Inc.
120 Terminal Drive
Plainview, L. I., New York 11803
Attn: Service Department

PARTS LIST FOR COMPLETE 361

TSI Stock No.	Description	Qty	Schematic Number
A-1004	Input Amplifier	1	609-D-103
A-1006	Gating Logic	1	609-D-191
A-1007	Signal Divider	1	609-D-195
A-1002	100 KHz Fast Decade Readout #22	5	609-D-107
A-1003	1 MHz Decade Readout #21	1	609-D-106
A-1005	Time Base Generator	1	609-D-104
A-1009	1 MHz Oscillator	1	609-C-215
A-1008	Power Supply	1	609-C-132
	Front Panel Assembly and Chassis		609-E-144

PARTS LIST FOR INPUT AMPLIFIER 609-D-103- S

TSI PART NO. A-1004 COLOR-BLUE

Reference Designation	TSI Stock No.	Description	Manufacturer
C47, 49, 50, 51, 53 54, 56, 58, 59, 60 62, 63	C-1048	220 mmfd Disc Cap ± 10% 1KV	RMC
C48, 52, 57, 61	C-1019	.01 mfd Disc Cap ± 20% 250V	RMC
C2, 3, 4, 8, 9 10, 13	C-2001	100 mfd Electrolytic Cap 15V	Sprague
C5, 11, 46	C-3003	18 mfd Tantalum Cap 10% 15V	Sprague
C55	C-3005	180 mfd " " " "	Mallory
C1, 7	C-3008	2 mfd 150V " " " "	"

PARTS LIST FOR INPUT AMPLIFIER 609-D-103-S (cont.)

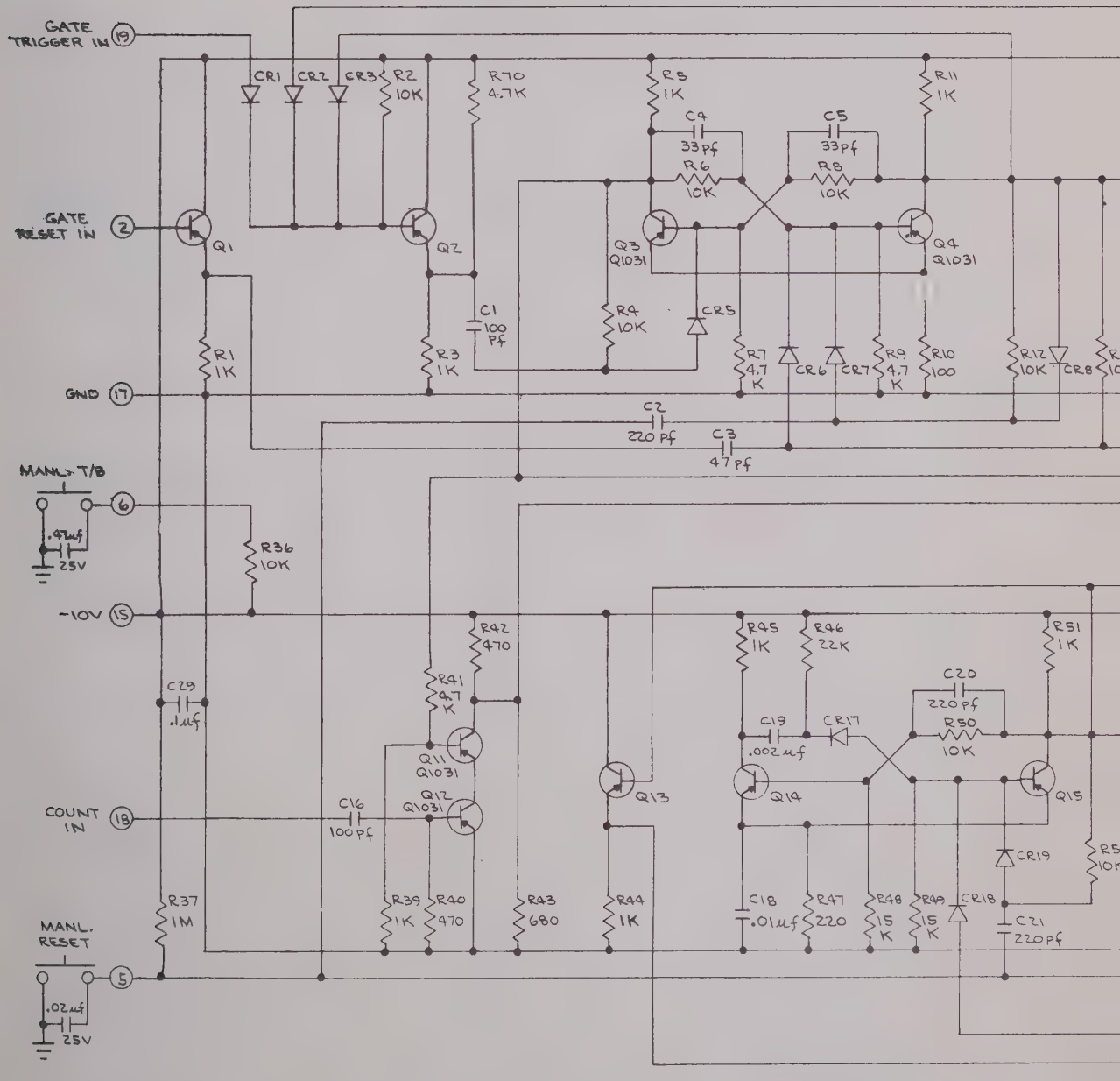
TSI PART NO. A-1004 COLOR-BLUE

Reference Designation	TSI Stock No.	Description	Manufacturer
C6, 12, 64, 65, 66	C-5705	47 pf DM-10-470J 5%	Elmenco
CR23 thru CR30	CR-1001	1N-191 Diode	ITT/SYL
Q21 thru Q28	Q-1001	TSI #700-B-02 Transistor 2N2929	G E
Q3, 4, 5, 6, 7, 8 11, 12, 13, 14, 15 16	Q-1031	Q-1031	Motorola
Q1, 2, 9, 10	Q-1048	2N-3638 "	Fairchild
R14, 36	R-1005	47 Ohm 1/2W 10 % Resistor	Allen Bradley
R5, 11, 27, 33, 49 50	R-1008	100 " " " "	" "
R20, 42, 98, 107 116, 125	R-1010	220 " " " "	" "
R10, 32	R-1011	330 " " " "	" "
R17, 39	R-1013	680 " " " "	" "
R12, 18, 19, 34 40, 41, 91, 95 101, 104, 109 113, 119, 122	R-1015	1K " " " "	" "
R22, 24	R-1016	1.5K " " " "	" "
R6, 13, 28, 35	R-1017	2.2K " " " "	" "
R16, 38	R-1019	4.7K " " " "	" "
R9, 31	R-1020	6.8K " " " "	" "
R7, 21, 29, 43, 94 99, 100, 102, 103 108, 112, 117, 118 120, 121, 126	R-1022	10K " " " "	" "
R96, 97, 105, 106 114, 115, 123, 124	R-1023	15K " " " "	" "
R93, 111	R-1024	22K " " " "	" "
R8, 30	R-1026-1	56K " " " "	" "
R3, 4, 25, 26	R-1029	100K " " " "	" "
R2, 24	R-1034	680K " " " "	" "
R1, 23	R-1036	1 meg. " " " "	" "
R92, 110	R-4004	10K 1/4W 10% Trimpot	Bourns
	TB-2002-1	For A-1004-R	T S I

PARTS LIST FOR GATING LOGIC (609-D-191-E)

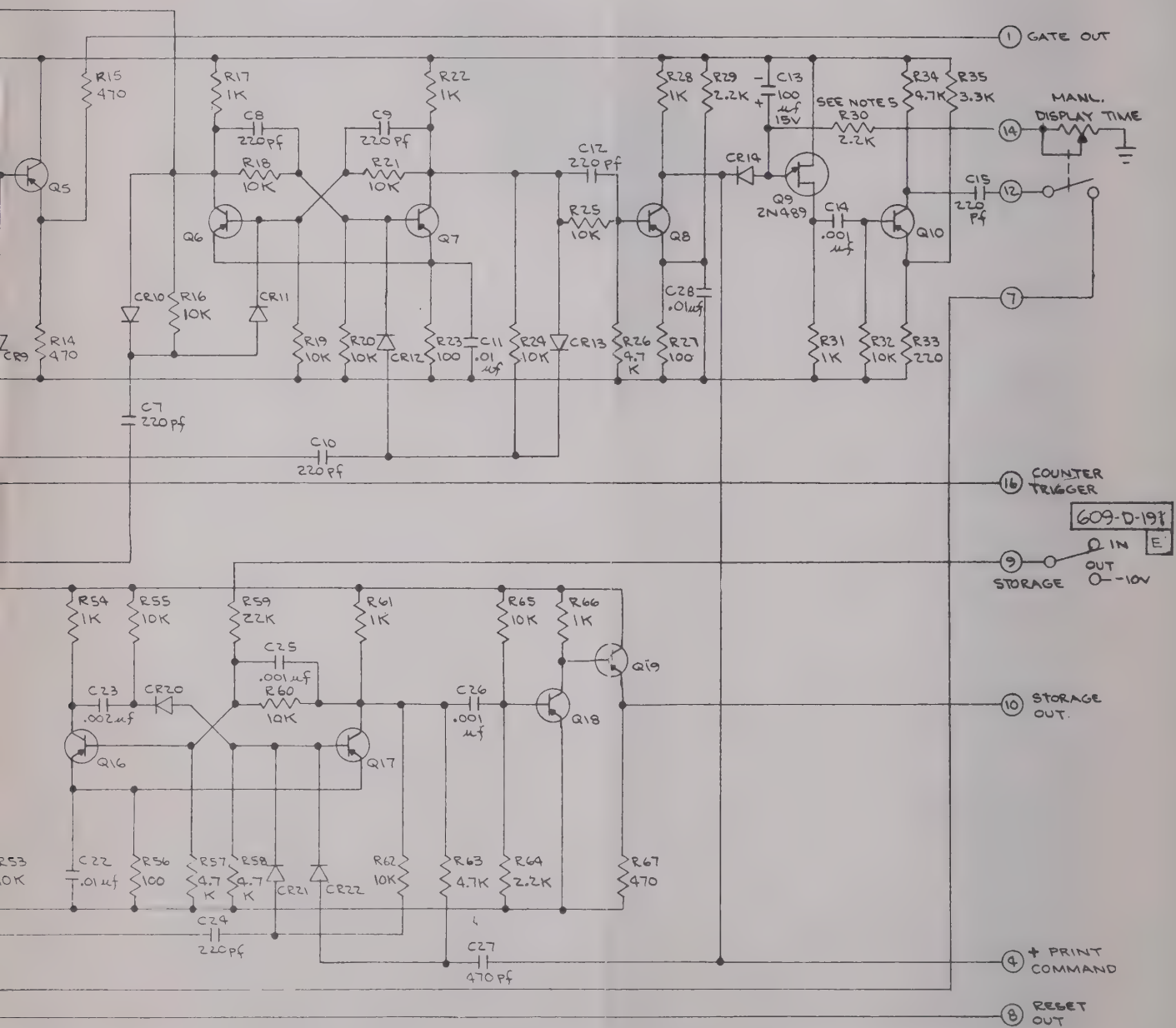
TSI PART NO. A-1006 COLOR-YELLOW

Reference Designation	TSI Stock No.	Description	Manufacturer
C4, 5	C-1043	33 pfd Disc Cap	RMC
C3	C-1044	47 " " "	"
C1, 16	C-1046	100 " " "	"
C2, 7, 8, 9, 10 12, 15, 20, 21 24	C-1048	220 " " "	"



NOTES:

1. ALL DIODES ARE IN191 UNLES
2. ALL TRANSISTORS ARE Q1001
3. ALL RESISTORS ARE ½W ±
4. PRINTED CKT. BD. 609-E-
5. R30 = 4.7K WHEN PRINTER



OTHERWISE SPECIFIED.
LESS OTHERWISE SPECIFIED.
:
.
ADOUT IS USED.

REQ'D	ITEM	PART NO	DESCRIPTION	MATERIAL	SPEC		WT	ZONE

LIST OF MATERIALS

		MATERIAL	TRANSISTOR SPECIALTIES, INC. PLAINVIEW, L.I., N.Y.					
		HEAT TREAT	TITLE GATING LOGIC					
		FINISH						
		BREAK ALL SHARP EDGES .010 R. MAX.	SCALE ~	DWN RW	4-3-64	DWG. NO. 609-D-191		
		TOLERANCES UNLESS SPECIFIED		CKD.				
		FRACT.±	ANGLES±	APP. RG	7-3-64	SHT. 1 OF	REV. E	
		DEC..00±	MACHINE FINISH					
NEXT ASSY	USED ON	DEC.000±	RMS MU IN					

PARTS LIST FOR GATING LOGIC (609-D-191-E) (cont.)

TSI PART NO. A-1006 COLOR-YELLOW

Reference Designation	TSI Stock No.	Description	Manufacturer
C27	C-1050	470 pfd Disc Cap	RMC
C14, 25, 26	C-1052	.001 mfd " "	"
C19, 23	C-1063	.002 mfd " "	"
C11, 18, 22, 28	C-1019	.01 mfd " "	"
C13	C-2001	100 mfd Electrolytic Cap 15V	Sprague
C29	C-1032	.1 mf	RMC
CR1, 2, 3, CR5 thru CR14, CR 17 thru CR22	CR-1001	1N-191 Diode	ITT/SYL
Q1, 2, 5, 6, 7, 8 10, 13, 14, 15, 16 17, 18, 19	Q-1001	TSI #700-B-02 Transistor 2N2929	G E
Q9	Q-1004	2N-489 Transistor	G E
Q3, 4, 11, 12	Q-1031	Q-1031 Transistor	Motorola
R10, 23, 27, 56	R-1008	100 Ohm 1/2W 10 % Resistor	Allen Bradley
R33, 47	R-1010	220 " " " "	" "
R14, 15, 40, 42, 67	R-1012	470 " " " "	" "
R43	R-1013	680 " " " "	" "
R1, 3, 5, 11, 17, 22 28, 31, 39, 44, 45 51, 54, 61, 66	R-1015	1K " " " "	" "
R29, 30, 64	R-1017	2.2K " " " "	" "
R35	R-1018	3.3K " " " "	" "
R7, 9, 26, 34 41, 57, 58, 63 70	R-1019	4.7K " " " "	" "
R2, 4, 6, 8, 12 13, 16, 18, 19 20, 21, 24, 25 32, 36, 50, 52 53, 55, 60, 65 62	R-1022	10K " " " "	" "
R48, 49	R-1023	15K " " " "	" "
R46, 59	R-1024	22K " " " "	" "
R37	R-1036	1 meg. " " " "	" "
	TB-2004	609-E-189 P.C. Board W/J-1004 Installed	T S I

PARTS LIST FOR SIGNAL DIVIDER(609-D-195)

TSI PART NO. A-1007-R COLOR-WHITE

Reference Designation	TSI Stock No.	Description	Manufacturer
C25, 26, 30, 31 35, 36, 43, 44	C-1043	33 mmfd Disc Cap	RMC
C27, 28, 32, 34, 37 38, 41, 46	C-1044	47 mmfd Disc Cap ± 10% 1KV	RMC
C40	C-1047	150 mmfd Disc Cap ± 10% 1KV	RMC
C20, 22, 42	C-1048	220 mmfd Disc Cap ± 10% 1KV	RMC
C21, 23	C-1019	.01 mfd Disc Cap ± 20% 250V	RMC
C24	C-3002	1.8 mfd Tantalum Cap 15V	Sprague
CR20, 21, 22, 24 25, 26, 29, 30, 31 33, 35, 36, 40	CR-1001	1N-191 Diode	ITT/SYL
Q16, 18, 20, 21 31	Q-1001	TSI #700-B-02 Transistor 2N2929	G E
Q17, 19, 23, 24, 25 26, 27, 28, 29, 30 32	Q-1031	Q-1031 Transistor	Motorola
L1	E-2001	10 mH Choke	Stanwyck/Delevan
R50, 55, 68, 77 87, 91, 100	R-1008	100 Ohm 1/2W 10% Resistor	Allen Bradley
R56, 57, 58	R-1012	470 " " " "	" "
R104	R-1013	680 " " " "	" "
R47, 49, 51, 53 61, 67, 71, 76 81, 86, 90, 94 99, 103	R-1015	1K " " " "	" "
R62, 69, 70, 78, 80 89, 93, 101	R-1018	3.3K " " " "	" "
R48, 54, 64, 66 72, 74, 83, 85 88, 92, 96, 98	R-1019	4.7K " " " "	" "
R46, 52, 63, 65, 73 75, 82, 84, 95, 97	R-1022	10K " " " "	" "
R79	R-1023	15K " " " "	" "
	TB-2005	609-E-196 P.C. Board W/J-1004 Installed	T S I

PARTS LIST FOR FAST 100 KHz DECADE BOARD #22 (609-D-107-G)

TSI PART NO. A-1002 COLOR-RED

Reference Designation	TSI Stock No.	Description	Manufacturer
C3, 4, 5, 6, 8, 9 10, 11, 13, 14 15, 16, 18, 19 20, 21	C-1048	220 mmfd Disc Cap ± 10% 1KV	RMC/Aerovox
C23	C-1051	680 mmfd Disc Cap ± 20% 1KV	RMC/Aerovox
C1, 2, 7, 12 17, 22	C-1019	.01 mfd Disc Cap ± 20% 250V	" "
CR1 thru CR7 CR9, 12, 13, 14 15, 17, 18, 19 24	CR-1001	1N-191 Diode	ITT/Sylvania
Q1 thru Q9	Q-1001	TSI #700-B-02 Transistor 2N2929	G E
Q10 thru Q19	Q-1002	TSI #700-B-01 Transistor 2N1893	T. S. I. Amperex Fairchild
R13, 23, 31, 40	R-1010	220 Ohm 1/2W 10% Resistor	Allen Bradley
R3	R-1011	330 " " " "	" "
R6, 7, 15, 16, 24 26, 33, 34	R-1015	1K " " " "	" "
R1, 2	R-1019	4.7K " " " "	" "
R8, 9, 10, 11, 12 14, 18, 19, 20, 21 22, 26, 27, 28, 29 30, 32, 35, 36, 37 38, 39, 41, 42, 17	R-1022	10K " " " "	" "
R52 thru R66	R-1023	15K " " " "	" "
R43 R48 thru 51 R67, thru R82	R-1024	22K " " " "	" "
R5	R-1025	33K " " " "	" "
R83	R-1026-1	56K " " " "	" "
R4	R-1029	100K " " " "	" "
R94 thru 103	R-1036	1 meg. " " " "	" "
R84 thru R93	R-1038	2.2 meg. " " " "	" "
R46	R-1508-1	120 " " 5% "	" "
R47	R-1509-1	200 " " 5% "	" "
	TB-2001	609-D-102 P.C. Board W/J-1004 Installed	T. S. I.

PARTS LIST FOR 1 MHz DECADE BOARD #21 (609-D-106- G)

TSI PART NO. A-1003 COLOR-ORANGE

Reference Designation	TSI Stock No.	Description	Manufacturer
C5, 6, 10, 11, 15 16, 20, 21	C-1043	33 mmfd Disc Cap ± 10% 1KV	RMC
C3, 4, 8, 9, 13 14, 18, 19	C-1044	47 mmfd Disc Cap ± 10% 1KV	RMC
C26	C-1047	150 " " " " "	"
C1, 2	C-1019	.01 mfd " " " "	"
CR1 thru CR21 CR24	CR-1001	1N-191 Diode	ITT/SYL
Q1	Q-1001	TSI #700-B-02 Transistor 2N2929	T. I.
Q10 thru Q19	Q-1002	TSI #700-B-01 " 2N1893	T. I. /Amperex Fairchild
Q2 thru Q9	Q-1031	SM/232	Motorola
R13, 23, 31, 40	R-1008	100 Ohm 1/2W 10 % Resistor	Allen Bradley
R3	R-1011	330 " " " "	" "
R42	R-1012	470 " " " "	" "
R6, 7, 13, 16 24, 25, 33, 34	R-1015	1K " " " "	" "
R12, 14, 21, 22 30, 32, 39, 41	R-1018	3.3K " " " "	" "
R1, 2, 10, 11, 19 20, 28, 29, 37 38, 43	R-1019	4.7K " " " "	" "
R8, 9, 17, 18, 26 27, 35, 36	R-1022	10K " " " "	" "
R52 thru R66	R-1023	15K " " " "	" "
R48 thru R51 R67 thru R82	R-1024	22K " " " "	" "
R5	R-1025	33K " " " "	" "
R83	R-1026-1	56K " " " "	" "
R4	R-1029	100K " " " "	" "
R94 thru R103	R-1036	1 meg. " " " "	" "
R84 thru R93	R-1038	2.2 meg. " " " "	" "
R46	R-1508-1	120 Ohm " 5% "	" "
R47	R-1511	330 " " " "	" "
	TB-2001	609-D-102- P. C. Board W/J-1004 Installed	T. S. I.

PARTS LIST FOR TIME BASE GENERATOR(609-D-104-E)

TSI PART NO. A-1005 COLOR-VIOLET

Reference Designation	TSI Stock No.	Description	Manufacturer
C2	C-1043	33 pfd Disc Cap	RMC
C4	C-1044	47 mmfd Disc Cap ± 10% 1KV	RMC
C5, 6, 8, 9, 11 13, 14, 15, 17 18, 20, 22, 23 24, 26, 27, 29 31, 32, 33, 35 36, 38, 40, 41 42, 44, 45	C-1048	220 mmfd Disc Cap 1KV ± 10%	RMC/Aerovox
C7, 12, 16, 21, 25 30, 34, 39, 43	C-1019	.01 mfd Disc Cap ± 20% 250V	RMC
C37	C-3002	1.8 mfd Tantalum Cap ± 10% 15V	Sprague
C28	C-3006	2 mfd D.P. Cap ± 10% 100V	Sprague
C19	C-3007	.02 mfd D.P. Cap ± 10% 100V	Elmenco/Sangamo
C1	C-5709-3	200 pfd DM-10-201 J 5%	" "
C10	C-5716-1	1800 pfd DM-19-182 K 10%	" "
CR1, 2, 4, 5, 6, 7 8, 9, 10, 11, 12, 13 14, 15, 16, 17, 18 19, 20, 21, 22, 23	CR-1001	1N-191 Diode	ITT/SYL
Q3 thru Q20	Q-1001	TSI #700-B-02 Transistor 2N2929	G E
Q1, 2	Q-1031	Q-1031 Transistor	Motorola
R8, 17	R-1008	100 Ohm 1/2W 10% Resistor	Allen Bradley
R26, 35, 44, 53 62, 71, 80, 89	R-1010	220 " " " "	" "
R1, 5, 11, 14, 19 23, 29, 32, 37, 41 46, 49, 55, 59, 65 68, 73, 77, 83, 86	R-1015	1K " " " "	" "
R6	R-1019	4.7K " " " "	" "
R9	R-1020	6.8K " " " "	" "
R4, 7, 10, 12 13, 15, 16, 18 22, 27, 28, 30 31, 33, 34, 36 40, 45, 47, 48 50, 51, 52, 54 58, 63, 66, 67 64, 69, 70, 72 76, 81, 82, 84 85, 87, 88, 90	R-1022	10K " " " "	" "
R24, 25, 42, 43 60, 61, 78, 79	R-1023	15K " " " "	" "
R3, 21, 39, 57 75	R-1024	22K " " " "	" "
R2, 20, 38, 56 74	R-4004	10K Trimpot 1/4W 10% Resistor	Bourns
	TB-2003	609-D-104- P.C. Board W/J-1004 Installed	T.S.I.

PARTS LIST FOR OSCILLATOR AND PRINT COMMAND(609-C-215-A)

TSI PART NO. A-1009 and A-1009-1 COLOR-BLUE

NOTE

This parts list is divided into three sections. The first section is for instruments which contain the 1 MHz oscillator but do not have storage or printer output capability. The second section contains the parts associated with storage. The third section contains the parts associated with printer output option.

Reference Designation	TSI Stock No.	Description	Manufacturer
C12, 14, 15	C-1052	.001 mfd Disc Cap ± 20% 1KV	RMC
C10, 13	C-5315	1000 pfd DM-15	Elmenco/Sangamo
C11	C-5708	100 pfd DM-10 ± 5%	Elmenco/Sangamo
L1	E-3010	25 mh Vari Choke	Caddell/Burns
Q9, 10	Q-1001	TSI #700-B-02 Hi Beta Transistor 2N2929	G E
Q7, 8	Q-1043	2N-3638 Transistor	Fairchild
R31	R-1005	47 Ohm 1/2W 10% Resistor	Allen Bradley
R29	R-1008	100 " " " "	" "
R22	R-1011	330 " " " "	" "
R28	R-1015	1K " " " "	" "
R25	R-1017	2.2K " " " "	" "
R24	R-1019	4.7K " " " "	" "
R26	R-1022	10K " " " "	" "
R21, 23	R-1024	22K " " " "	" "
R27	R-1029	100K " " " "	" "
R30	R-2010	220 " 1W " "	" "
	TB-2168	609-D-210 P.C. Board W/J-1004 Installed	T.S.I

NOTE

The second section of the parts list covers the components associated with storage capability.

C1	C-1062	.003 Mf mfd Disc Cap	RMC
C2, 3	C-1048	220 pf mfd Disc Cap ± 10% 1KV	RMC/Aerovox
CR1	CR-1001	1N-191 Diode	ITT/SYL
Q1, 2	Q-1032	2N-404	R C A

PARTS LIST FOR OSCILLATOR AND PRINT COMMAND (609-C-215-A) (cont.)

TSI PART NO. A-1009 and A-1009-1 COLOR-BLUE

Reference Designation	TSI Stock No.	Description	Manufacturer
R1, 7	R-1018	3.3K 1/2W 10% Resistor	Allen Bradley
R2	R-1010	220 " " "	" "
R3	R-1024	22K " " "	" "
R4, 5	R-1019	4.7K " " "	" "
R6	R-1023	15K " " "	" "
		NOTE	
The third section of this list covers the components associated with printer output capability.			
C4, 6, 7	C-1048	220 mfd Disc Cap ± 10% 1KV	RMC/Aerovox
C5	C-1062	.003 Mf Disc Cap	RMC
C8, 9	C-1032	0.1 Mf Disc Cap 20%	RMC
CR2	CR-1001	1N-191 Diode	ITT/SYL
CR3	CR-2008	1N-712-A Diode	Dickson
CR4	CR-1010	G-382 ITT or D6639	ITT/SYL
Q3, 4, 5	Q-1032	2N-404	R C A
Q6	Q-1002	NIXIE DRIVER 2N1893	Amperex/Fairchild
R9	R-1010	220 Ohm 1/2W 10% Resistor	Allen Bradley
R17, 18	R-1015	1K " " "	" "
R14, 15	R-1017	2.2K " " "	" "
R8, 11, 13	R-1018	3.3K " " "	" "
R19	R-1019	4.7K " " "	" "
R12	R-1020	6.8K " " "	" "
R20	R-1022	10K " " "	" "
R10, 16	R-1023	15K " " "	" "

PARTS LIST FOR POWER SUPPLY BOARD (620-C-132-F)

TSI PART NO. A-1008-A W/S COLOR-BLACK

Reference Designation	TSI Stock No.	Description	Manufacturer
C1 thru C4	C-2006	100 mfd Electrolytic Cap 25V	Sprague
CR8	CR-1022	CER-72 Diode	Solitron Devices
CR9	CR-2003	1N-712-A	DIXON
CR5	CR-2014	1N-2033 Zener Diode	Transitron/T. I.

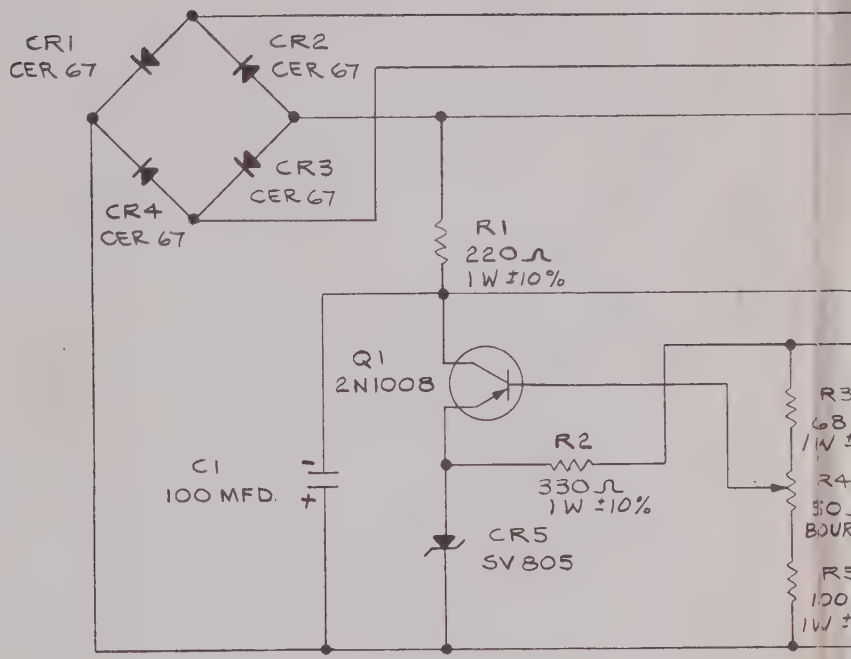
PARTS LIST FOR POWER SUPPLY BOARD (620-C-132-F) (cont.)

TSI PART NO. A-1008-A W/S COLOR-BLACK

Reference Designation	TSI Stock No.	Description	Manufacturer
CR1, 2, 3, 4	CR-2022	CER-67-Diode	Solitron Devices
Q1, 2	Q-1015	2N-1008 Transistor	Motorola
R6	R-1012	470 Ohm 1/2W 10% Resistor	Allen Bradley
R9	R-2003	22 " 1W " "	" "
R1	R-2010	220 " " " "	" "
R2	R-2011	330 " " " "	" "
R3	R-2506	68 " " 5% "	" "
R5	R-2508	100 " " " "	" "
R4	R-4017	50 " Trimpot	Bourns
	TB-2006	#620-C-168 Rev. P.C Board W/J-1004 Installed	TSI
		NOTE: THESE PARTS ARE USED FOR MODIFICATION M 30 (DISPLAY STORAGE)	
		Additional Parts for Storage	
C5	C-2006	100 mfd Electrolytic Cap 25V	Sprague
CR10	CR-1014	1N-714 Diode	Dickson
CR11	CR-2022	CER-67 Diode	Solitron Devices
Q3	Q-1002	TSI #700-B-01 Transistor 2N1893	Amperex Fairchild
R11	R-1015	1K 1/2W 10% Resistor	Allen Bradley
R10	R-1018	3.3K 1/2W 10% Resistor	" "

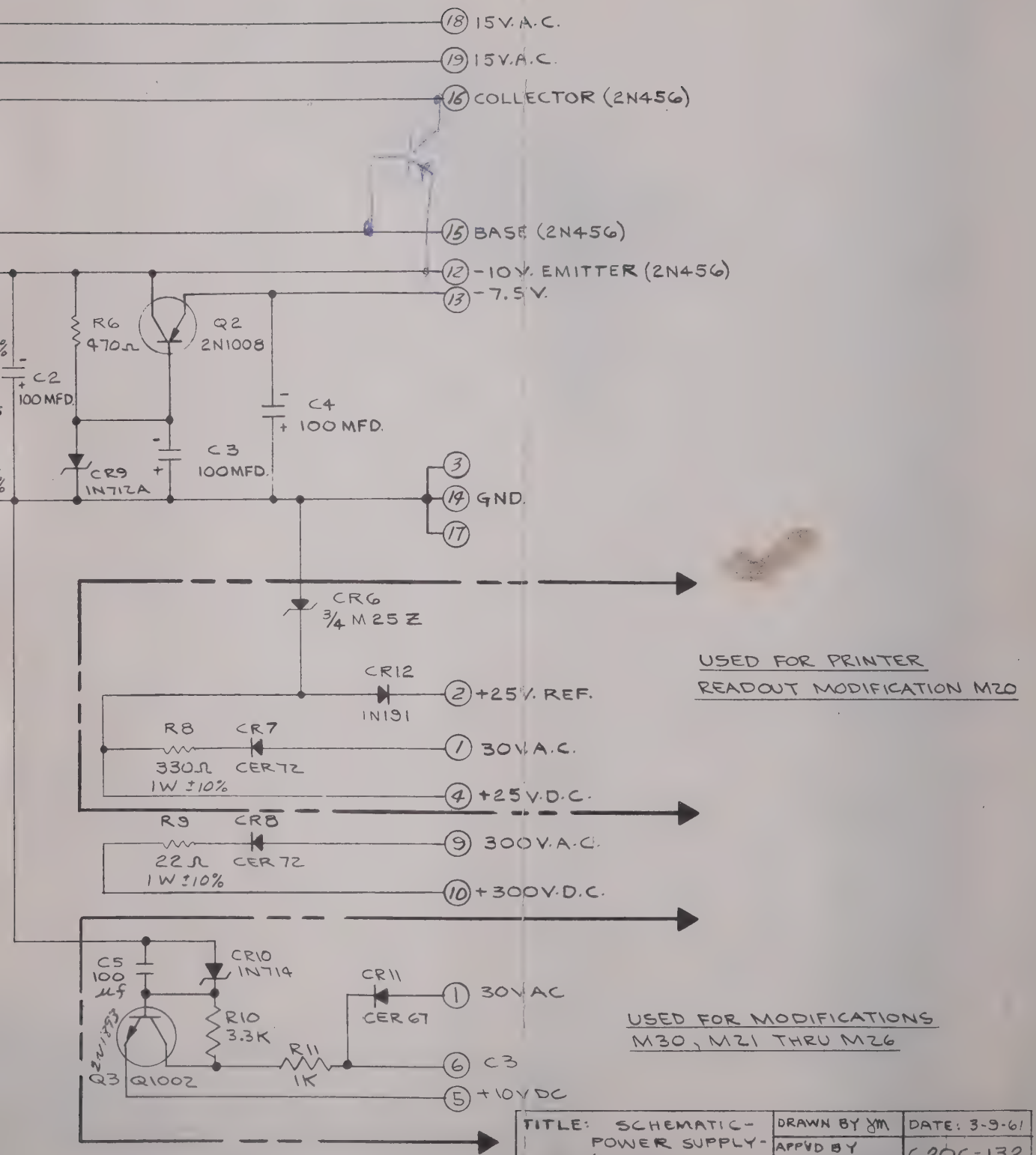
PARTS LIST FOR FRONT PANEL AND CHASSIS (609-E-144)

Reference Designation	TSI Stock No.	Description	Manufacturer
V1 thru V6	I-1001	Ultra Long Life Nixie Display Tube	Burroughs
S3, 4	S-2019	Rotary Switch 2 Pole 5 Pos.	Centralab
S6	S-2005	" " 4 Pole 6 Pos.	Centralab
S5	S-2013	Switch Rotary 9 Pos.	Centralab
J11, 12, 13	J-1001	BNC Connector	Dadge
S2	S-1005	Toggle Switch 3A 250V	Cutler Hammer
S7, 8	S-1010	Push Button Switch	Hetherington
S10	S-1015	Switch Attachable	Ohmite
R30	R-4014	Pot. .10 Meg	"
DS1	X-3003	Pilot Light	Dialight Corp.
R46, 47	R-1019	4.7K 1/2W 10% Resistor	Allen Bradley
C1	C-1022	Cap .47MF 25V	Sprague
R45, 48	R-4008	Pot 1500 2 W	Ohmite
R40	R-1023-1	18K 1/2W Resistor	Allen Bradley
C2	C-1020	.02 + 80 -20%	C R L



NOTE:

PRINTED CKT. BD. #620-C-168



TITLE: SCHEMATIC - POWER SUPPLY - 361 & 361-R	DRAWN BY XM	DATE: 3-9-61
	APP'D BY	620C-132
	CHK'D BY: DP	
TRANSISTOR SPECIALTIES INC.	SCALE: ~	REV: F

APPENDIX I
APTI-METER MODEL 361-R
(Rack-mounted Model)

GENERAL

This appendix describes and illustrates points of difference between Models 361 and 361-R. As noted in the Foreword, Model 361-R has been designed for mounting in a standard 19" rack. This has necessitated re-layout of components etc., resulting in a wholly different mechanical arrangement.

ELECTRICAL DESIGN

Apti-Meter Model 361-R is electrically identical to Model 361 described in the body of this instruction book. The theoretical description of electrical operation of Sections IV and V are wholly applicable. Electrical testing and trouble shooting as discussed in Section VII for Model 361 is identical for Model 361-R except for discussions of component, printed board, and adjustment locations. Tests and trouble shooting methods and procedures are identical to the methods and procedures described.

PHYSICAL DIFFERENCES

Figure 7-3A (page 7-9) is a top view of Apti-Meter Model 361-R. The printed boards are shown tilted and locked in position for servicing (see below). Installed position of the boards is illustrated in Figure 7-3B.

As can be seen in Figures 7-3B and 7-3E, the power supply and oscillator components have been arranged in a horizontal configuration to suit the low profile of the 361-R. However, the circuits used are identical to those in the Model 361, and the schematic diagram (609D130, Page 7-18) applies to both models. The illustrations of of the Power Supply Board and Oscillator Board have been repeated as Figures 7-3C and 7-3D, for convenience.

OPERATION

Apti-Meter Model 361-R is functionally and operationally identical to Model 361. As shown in Figure 3-4, and also 7-3A, front panel controls have been rearranged, but all controls are identical in function and marking to those of Model 361. Operating procedures given in Section III of this instruction book are wholly applicable to both models.

In terms of performance also, identical specifications apply. The discussion of functional modes of Section III pertains equally to both models. Figure 7-3C locates the GATE OUT connector and illustrates as well the location of the printer readout connector described in Appendix II.

OSCILLATOR ADJUSTMENT

The oscillator trimmer capacitor adjustment used to standardize the oscillator frequency against WWV or a primary standard (See Section VI) is located as shown in figure 7-3E. This capacitor is adjusted, using a long, thin tuning wand, from behind the Apti-Meter. It is not necessary to remove covers to make this adjustment. The methods of adjusting oscillator frequency are fully described in Section VI and are applicable to both Models. The tuning wand may be observed to engage the capacitor slot, after passing through the rear panel hole, from above the unit.

–10 VOLT ADJUSTMENT

The location of the –10 volt regulated power supply adjustment is shown in figures 7-3C and 7-3E. This is a potentiometer adjustment identical to that previously described. Access to this potentiometer is provided by a hole drilled on the right side of the unit about 3" from the rear plate.

TIME BASE ADJUSTMENT

Figure 7-3E locates the Time Base Potentiometer adjustments. These are accessible from the top of the unit and, when facing the instrument, are, from right to left: 10 CPS – 100 CPS – 1 Kc – 10 Kc and 100 Kc on the first board and 1 CPS and 0.1 CPS on the fourth board. Adjustment of these potentiometers is described in Section VII. The potentiometers are mounted on printed boards 609D-105A and 609D103 (See figure 7-3E) which must be in the position shown for accessibility of the potentiometer (see below).

INPUT ATTENUATOR ADJUSTMENT

Adjustment of the input attenuators is fully described in the instruction book for Model 361. Model 361-R input circuitry is identical to that of the bench model and operation of the attenuators is exactly the same. The attenuator adjustments in Model 361-R are located as shown in figure 7-3B. Facing the unit, the attenuator adjustments for Channel B are to the left of those of Channel A; both are to be found in the front right corner of the instrument. The attenuator trimmer associated with each attenuator is clearly shown in the illustration (figure 7-3B).

PRINTED BOARD ACCESS

The printed boards of Model 361-R are mounted in two frames referred to here as the right and left frame looking down on the instrument from the front. The left frame (see figure 7-3E) mounts boards 609D106, 609D107 and three of 609D102. The right frame mounts 609D105A, 609-D104, 609D105B and 609D103. This sequence is given in each case from top to bottom with the boards in operating position.

Each frame is hinged to permit the boards to be positioned for easy accessibility. Figure 7-3E illustrates the boards in maintenance position and this is also illustrated in figure 7-3A, in this case in an intermediate position. Each frame with its complement of boards may tilted as follows:

1. Loosen small knurled bolts located on board support part (see figure 7-3B).
2. Loosen the two knurled bolts along edges of board.
3. Swing board assembly upward until movable part clears knurled knob.
4. Push knurled knob in.
5. Board assembly will remain in tilted position.

The individual boards are removed by drawing them clear of the mating receptacles.

ADDENDUM

FOR MODEL 361R/M30

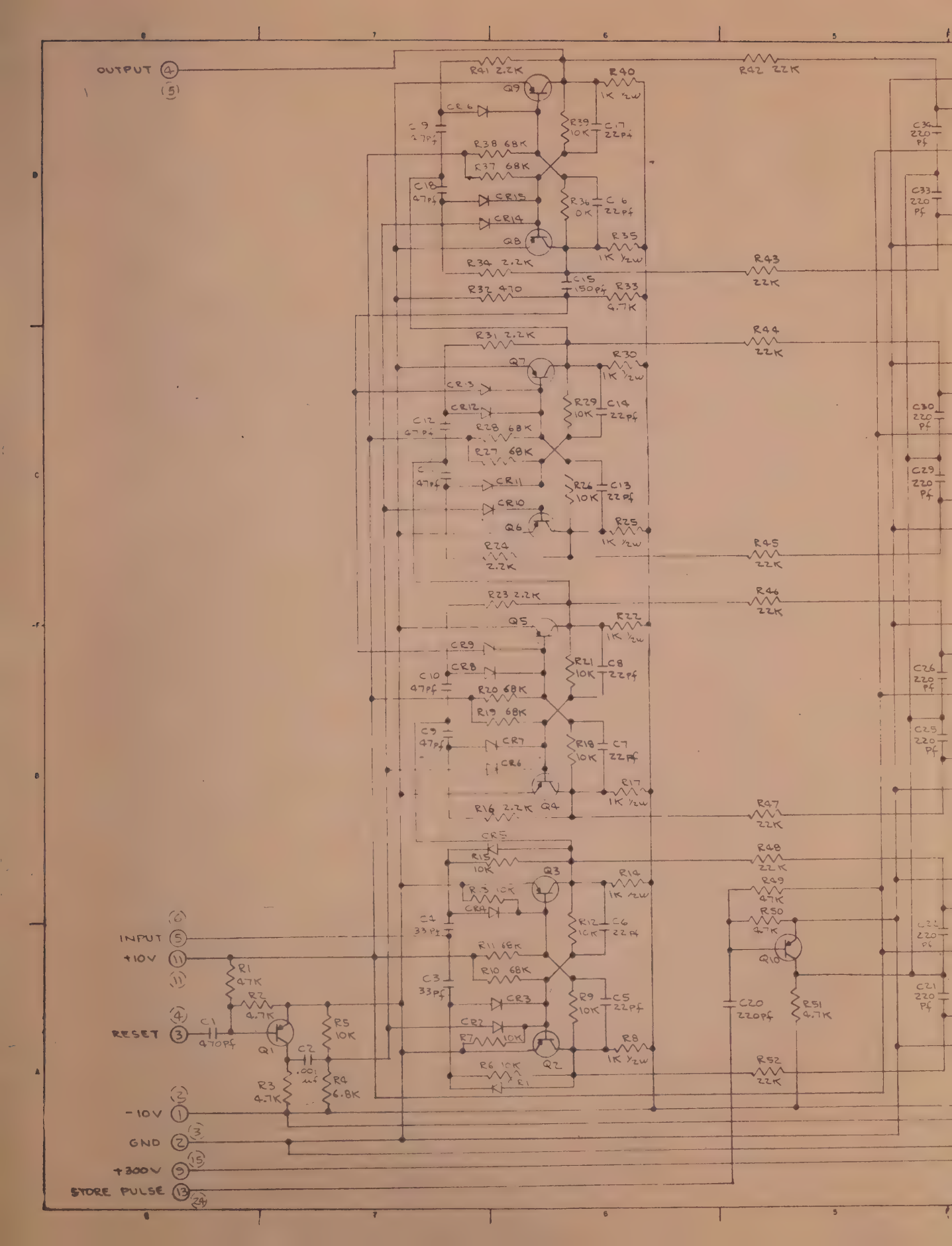
This addendum covers the additional features contained in the Model 361R/M30 which is not contained in the Model 361R Manual.

M30 DISPLAY STORAGE

This feature is enabled when the STORAGE switch on the back of the unit is in the STORAGE IN position. In the STORAGE IN position the display does not change unless the new count differs from the previous count and only the digits that are to be updated are changed. This permits the operator to set the DISPLAY TIME control at lower values, since the display reading is held on during succeeding measurements. In addition the STORAGE feature reduces operator fatigue when long monitoring periods are required.

The circuitry for the DISPLAY STORAGE contains a monostable multivibrator that triggers at a rate set by the DISPLAY TIME control with the switch in the STORAGE IN position.

When the switch is moved to the STORAGE OUT position the multivibrator freeruns at a 50 KHz rate. Since 50 KHz is faster than the human eye can detect, it appears as if the NIXIE tubes are incrementing for each input pulse. The storage decades therefore appear to be following the counting decades at all times. This mode is useful when the TRIGGER LEVEL is being set, since the triggering point will be shown by the counting process. (Note until the triggering point is reached, counting will not occur. In the STORAGE IN mode the display would appear as a very stable count.) In addition if the count is slow or over a long period of time, the STORAGE OUT mode will show how the count is proceeding and corrective action can be taken.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INPUT
+10V
RESET
-10V
GND
+300V
STORE PULSE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
R1 4.7K
R2 4.7K
R3 4.7K
R4 6.8K
R5 10K
C1 470pf
C2 .001 mf
R6 10K
R7 10K
R8 1K ½w
R9 10K
C5 22pf
R10 68K
R11 68K
R12 10K
C6 22 pf
C3 33pf
R13 10K
R14 1K ½w
CR4
C4 33 Pf
R15 10K
CR5
R16 2.2K
R17 1K ½w
R18 10K
C7 22pf
CR6
CR7
C9 47pf
R19 68K
R20 68K
R21 10K
C8 22pf
CR8
CR9
C10 47pf
R22 1K ½w
R23 2.2K
R24 2.2K
R25 1K ½w
R26 10K
C13 22pf
CR10
CR11
C11 47pf
R27 68K
R28 68K
R29 10K
C14 22pf
CR12
CR13
C12 47pf
R30 1K ½w
R31 2.2K
R32 470
R33 4.7K
C15 150pf
R34 2.2K
R35 1K ½w
R36 10K
C16 22pf
CR14
CR15
C18 47pf
R37 68K
R38 68K
R39 10K
C17 22pf
CR16
C19 47pf
R40 1K ½w
R41 2.2K
R42 22K
R43 22K
R44 22K
R45 22K
R46 22K
R47 22K
R48 22K
R49 47K
R50 47K
R51 4.7K
R52 22K
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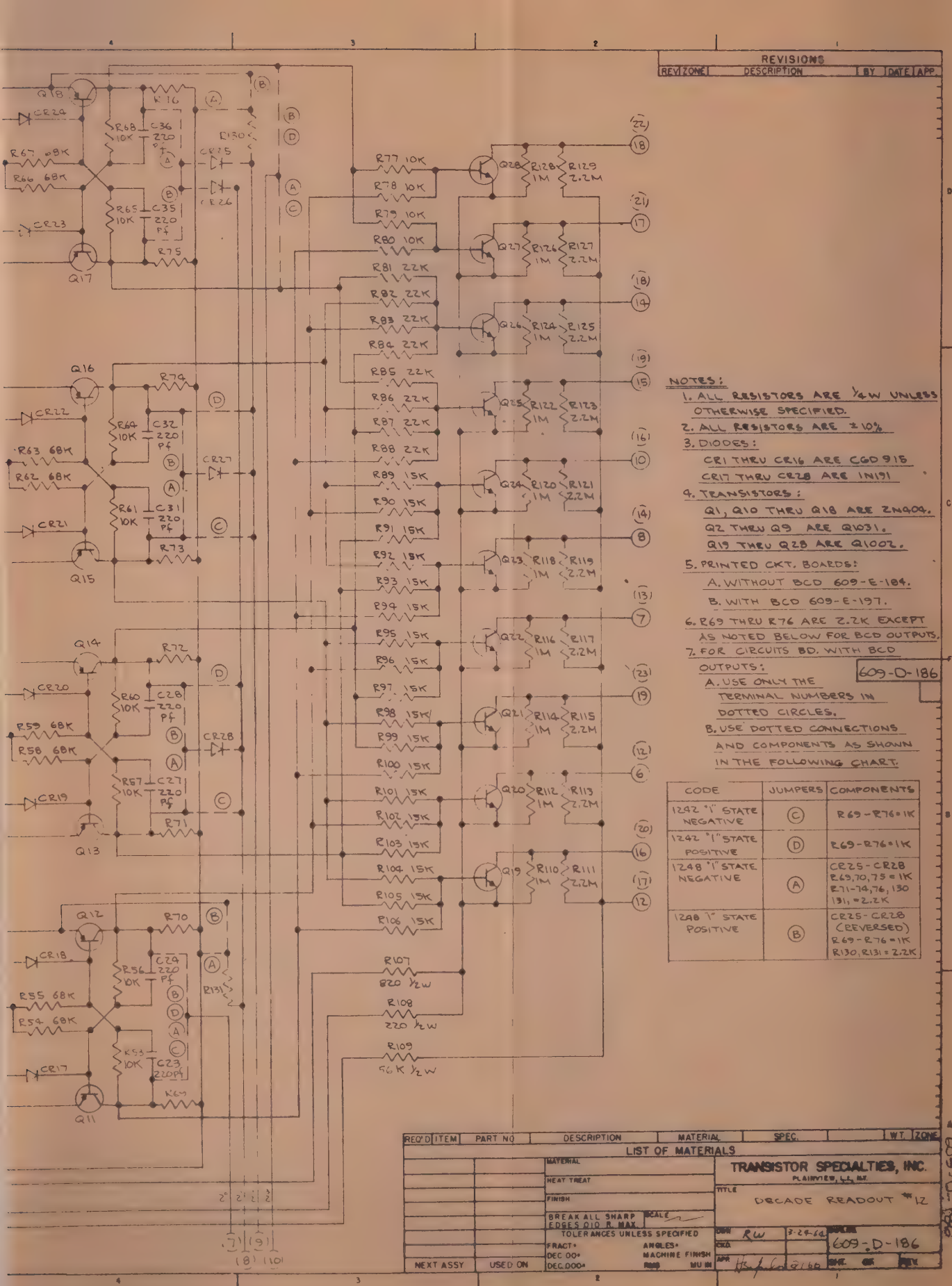
C22 220 pf
C25 220 Pf
C26 220 pf
C29 220 Pf
C30 220 pf
C33 220 Pf
C34 220 pf


REVISIONS
REV ZONE | DESCRIPTION | BY | DATE | APP.
Q18
CR24
R68 10K
C36 220 Pf
R67 68K
R66 68K
R65 10K
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Q17
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R130
CR25
CR26
Q16
R74
CR22
R64 10K
C32 220 Pf
R63 68K
R62 68K
R61 10K
C31 220 Pf
CR21
Q15
R73
CR27
Q14
R72
CR20
R60 10K
C28 220 Pf
R59 68K
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R57 10K
C27 220 Pf
CR19
Q13
R71
CR28
Q12
R70
CR18
R56 10K
C24 220 Pf
R55 68K
R54 68K
R53 10K
C23 220Pf
CR17
Q11
R69
R131
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R79 10K
R80 10K
R81 22K
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R88 22K
R89 15K
R90 15K
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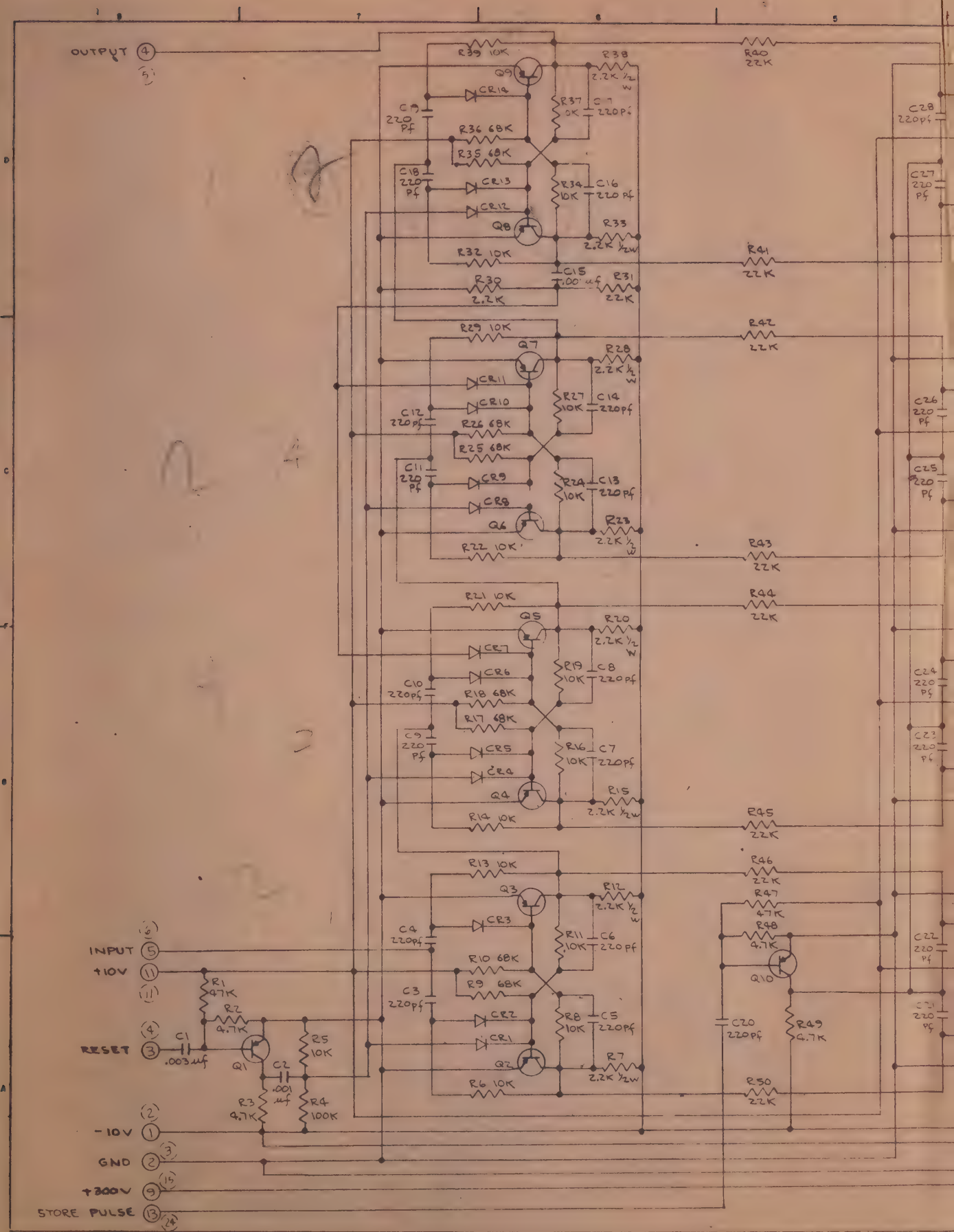
R92 15K
R93 15K
R94 15K
R95 15K
R96 15K
R97 15K
R98 15K
R99 15K
R100 15K
R101 15K
R102 15K
R103 15K
R104 15K
R105 15K
R106 15K
R107 820 1/2W
R108 220 1/2W
R109 56K 1/2W
Q28 R128 1M R129 2.2M
Q27 R126 1M R127 2.2M
Q26 R124 1M R125 2.2M
Q25 R122 1M R123 2.2M
Q24 R120 1M R121 2.2M
Q23 R118 1M R119 2.2M
Q22 R116 1M R117 2.2M
Q21 R114 1M R115 2.2M
Q20 R112 1M R113 2.2M
Q19 R110 1M R111 2.2M
NOTES:
1. ALL RESISTORS ARE 1/4W UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE ±10%
3. DIODES:
CR1 THRU CR16 ARE CGD 918
CR17 THRU CR28 ARE IN191
4. TRANSISTORS:
Q1, Q10 THRU Q18 ARE 2N404.
Q2 THRU Q9 ARE Q1031.
Q19 THRU Q28 ARE Q1002.
5. PRINTED CKT. BOARDS:
A. WITHOUT BCD 609-E-184.
B. WITH BCD 609-E-197.
6. R69 THRU R76 ARE 2.2K EXCEPT AS NOTED BELOW FOR BCD OUTPUTS.
7. FOR CIRCUITS BD. WITH BCD OUTPUTS: 609-D-186
A. USE ONLY THE TERMINAL NUMBERS IN DOTTED CIRCLES.
B. USE DOTTED CONNECTIONS AND COMPONENTS AS SHOWN IN THE FOLLOWING CHART.
CODE | JUMPERS | COMPONENTS
1242 "1" STATE NEGATIVE | C | R69-R76=1K
1242 "1" STATE POSITIVE | D | R69-R76=1K
1248 "1" STATE NEGATIVE | A | CR25-CR28 R69,70,75=1K R71-74,76,130 131,=2.2K
1248 "1" STATE POSITIVE | B | CR25-CR28 (REVERSED) R69-R76=1K R130,R131=2.2K
REQ'D | ITEM | PART NO | DESCRIPTION | MATERIAL | SPEC. | WT. | ZONE
LIST OF MATERIALS
MATERIAL
HEAT TREAT
FINISH
BREAK ALL SHARP EDGES .010 R MAX
TOLERANCES UNLESS SPECIFIED
FRACT± DEC .00± DEC .000±
ANGLES± MACHINE FINISH
NEXT ASSY | USED ON
TRANSISTOR SPECIALTIES, INC.
PLAINVIEW, L.I., N.Y.
TITLE DECADE READOUT *12
DWN RW 3-29-68
CKD
APP
SIZE 609-D-186
SHT OF REV
609-D-186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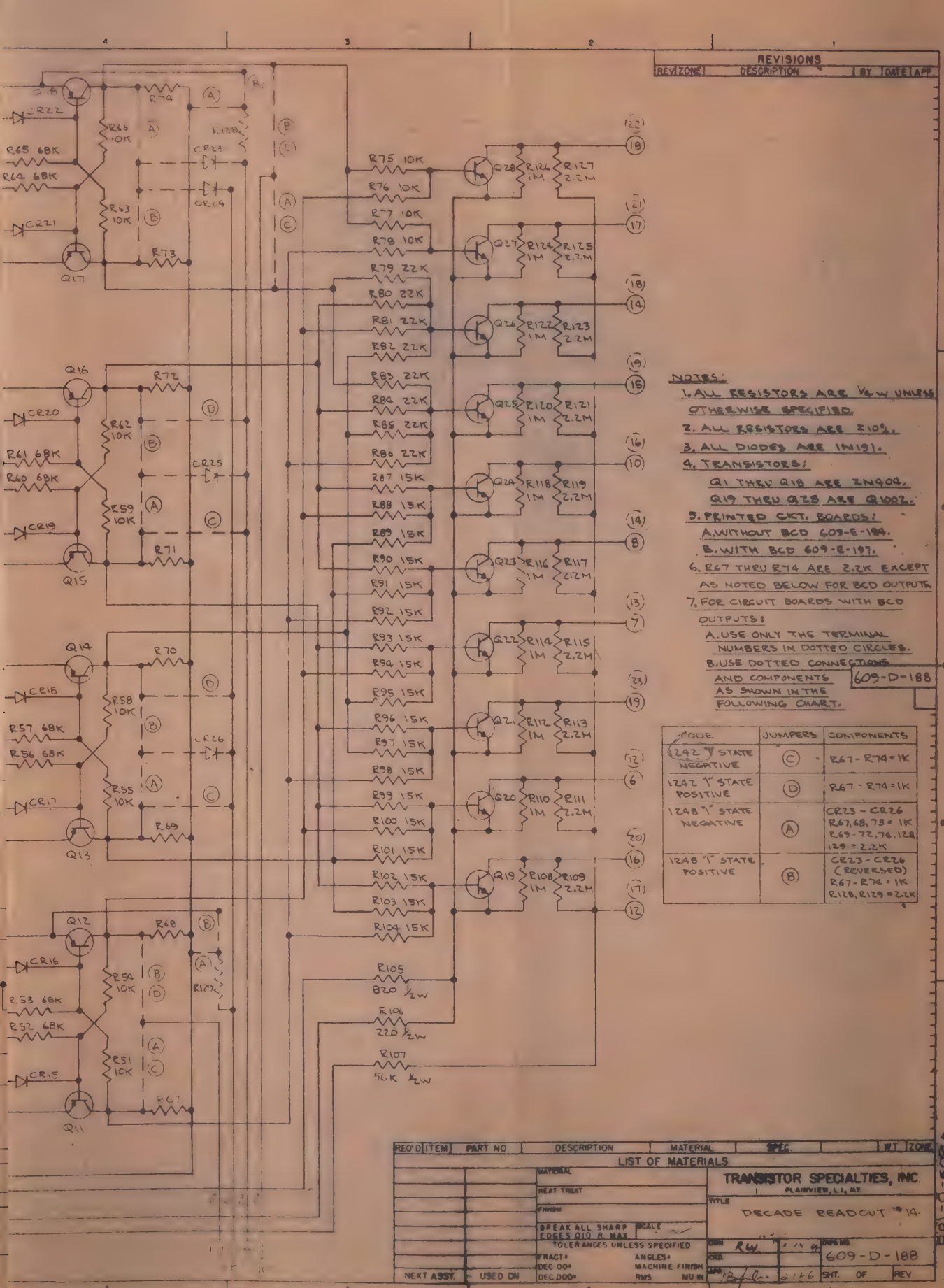
INPUT
+10V
RESET
-10V
GND
+300V
STORE PULSE
R1 47K
R2 4.7K
R3 4.7K
R4 100K
R5 10K
C1 .003 mf
C2 .001 mf
Q1
R6 10K
R7 2.2K ½W
Q2
R8 10K
C5 220pf
R9 68K
R10 68K
C3 220pf
CR1
CR2
R11 10K
C6 220 pf
R12 2.2K ½W
Q3
CR3
C4 220pf
R13 10K
R14 10K
R15 2.2K ½W
Q4
CR4
CR5
R16 10K
C7 220pf
R17 68K
R18 68K
C10 220pf
C9 220 Pf
R19 10K
C8 220 pf
R20 2.2K ½W
Q5
CR6
CR7
R21 10K
R22 10K
R23 2.2K ½W
Q6
CR8
CR9
R24 10K
C13 220 pf
R25 68K
R26 68K
C12 220pf
C11 220 Pf
R27 10K
C14 220pf
R28 2.2K ½W
Q7
CR10
CR11
R29 10K
R30 2.2K
R31 22K
C15 .100 mf
R32 10K
R33 2.2K ½W
Q8
CR12
CR13
R34 10K
C16 220 pf
R35 68K
R36 68K
C18 220 Pf
C17 220pf
R37 10K
R38 2.2K ½W
Q9
CR14
C19 220 Pf
R39 10K
R40 22K
R41 22K
R42 22K
R43 22K
R44 22K
R45 22K
R46 22K
R47 4.7K
R48 4.7K
Q10
C20 220pf
R49 4.7K
R50 22K
C28 220pf
C27 220 Pf
C26 220 Pf
C25 220 Pf
C24 220 Pf
C23 220 Pf
C22 220 Pf
C21 220 Pf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REV ZONE | DESCRIPTION | BY | DATE | APP.
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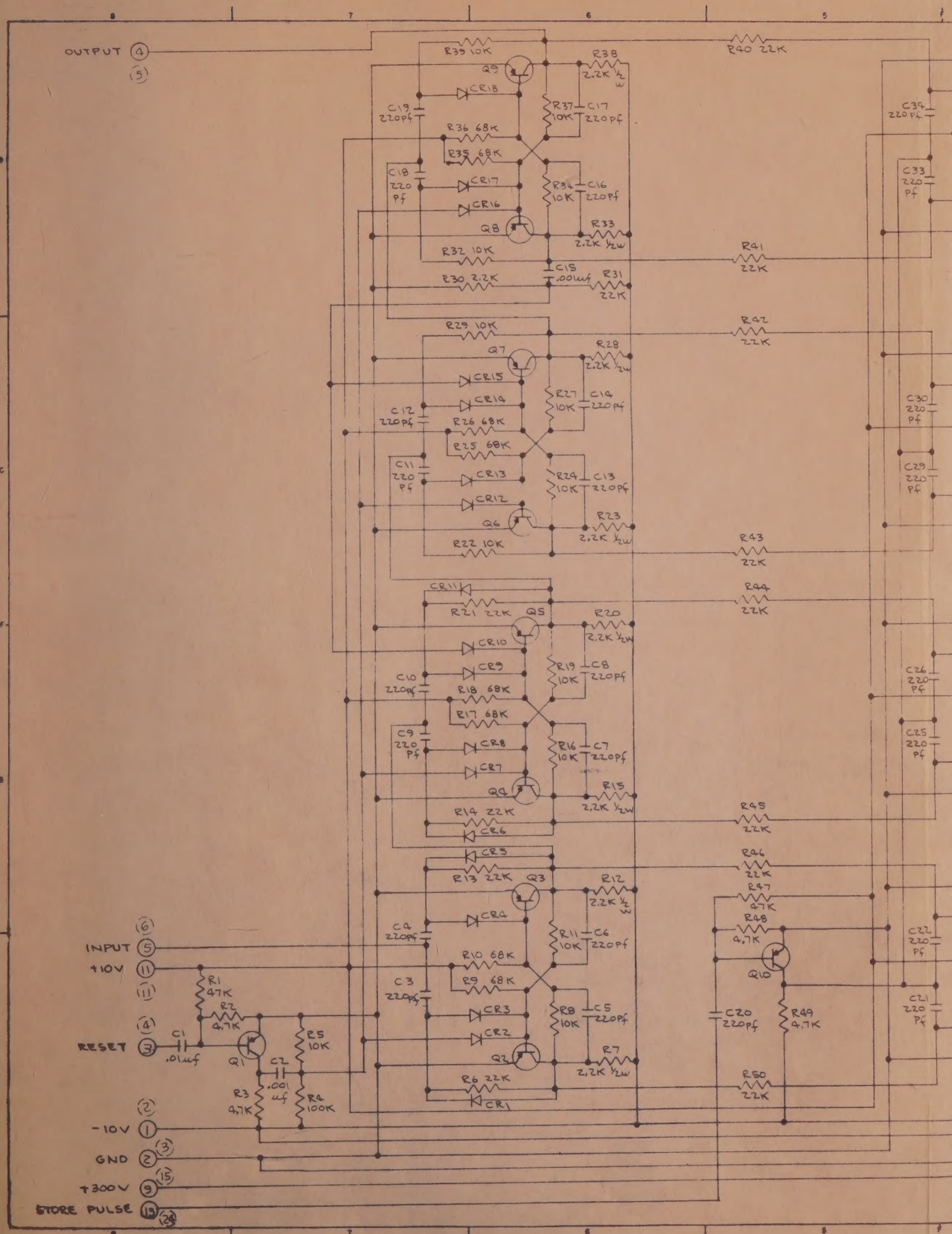
CR22
R66 10K
R65 68K
R64 68K
CR21
R63 10K
Q17
R74
R128
CR23
CR24
R73
Q16
R72
CR20
R62 10K
R61 68K
R60 68K
CR19
R59 10K
Q15
R71
CR25
Q14
R70
CR18
R58 10K
R57 68K
R56 68K
CR17
R55 10K
Q13
R69
CR26
Q12
R68
CR16
R54 10K
R53 68K
R52 68K
CR15
R51 10K
Q11
R67
R129
R75 10K
R76 10K
R77 10K
R78 10K
R79 22K
R80 22K
R81 22K
R82 22K
R83 22K
R84 22K
R85 22K
R86 22K
R87 15K
R88 15K
R89 15K
R90 15K
R91 15K
R92 15K
R93 15K
R94 15K
R95 15K
R96 15K
R97 15K
R98 15K
R99 15K
R100 15K
R101 15K
R102 15K
R103 15K
R104 15K
Q28 R126 1M R127 2.2M
Q27 R124 1M R125 2.2M
Q26 R122 1M R123 2.2M
Q25 R120 1M R121 2.2M
Q24 R118 1M R119 2.2M
Q23 R116 1M R117 2.2M
Q22 R114 1M R115 2.2M
Q21 R112 1M R113 2.2M
Q20 R110 1M R111 2.2M
Q19 R108 1M R109 2.2M
R105 820 ½W
R106 220 ½W
R107 56K ½W
NOTES:
1. ALL RESISTORS ARE ¼W UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE ±10%.
3. ALL DIODES ARE 1N191.
4. TRANSISTORS:
Q1 THRU Q18 ARE 2N404.
Q19 THRU Q28 ARE 2N697.
5. PRINTED CKT. BOARDS:
A. WITHOUT BCD 609-E-184.
B. WITH BCD 609-E-197.
6. R67 THRU R74 ARE 2.2K EXCEPT AS NOTED BELOW FOR BCD OUTPUTS.
7. FOR CIRCUIT BOARDS WITH BCD OUTPUTS:
A. USE ONLY THE TERMINAL NUMBERS IN DOTTED CIRCLES.
B. USE DOTTED CONNECTIONS AND COMPONENTS AS SHOWN IN THE FOLLOWING CHART.
609-D-188
CODE | JUMPERS | COMPONENTS
1242 "1" STATE NEGATIVE | C | R67 - R74 = 1K
1242 "1" STATE POSITIVE | D | R67 - R74 = 1K
1248 "1" STATE NEGATIVE | A | CR23 - CR26 R67, 68, 73 = 1K R69 - 72, 74, 128, 129 = 2.2K
1248 "1" STATE POSITIVE | B | CR23 - CR26 (REVERSED) R67 - R74 = 1K R128, R129 = 2.2K
REQ'D | ITEM | PART NO | DESCRIPTION | MATERIAL | SPEC. | WT | ZONE
LIST OF MATERIALS
MATERIAL
HEAT TREAT
FINISH
BREAK ALL SHARP EDGES .010 R. MAX.
SCALE
TOLERANCES UNLESS SPECIFIED
FRACT ± ANGLES ±
DEC .00 ± MACHINE FINISH
DEC .000 ± RMS MU IN
NEXT ASSY. | USED ON
TRANSISTOR SPECIALTIES, INC.
PLAINVIEW, L.I., N.Y.
TITLE
DECADE READOUT #14
DRN RW
CKD
APP
DWG NO. 609-D-188
SHT. OF REV
609-D-188


OUTPUT
INPUT
+10V
RESET
-10V
GND
+300V
STORE PULSE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
R1 47K
R2 4.7K
R3 4.7K
R4 100K
R5 10K
C1 .01uf
C2 .001 uf
C3 220pf
C4 220pf
R6 22K
R7 2.2K 1/2W
R8 10K
C5 220pf
R9 68K
R10 68K
R11 10K
C6 220pf
R12 2.2K 1/2 W
R13 22K
R14 22K
R15 2.2K 1/2W
R16 10K
C7 220pf
R17 68K
R18 68K
R19 10K
C8 220pf
R20 2.2K 1/2W
R21 22K
R22 10K
R23 2.2K 1/2W
R24 10K
C13 220pf
R25 68K
R26 68K
R27 10K
C14 220pf
R28 2.2K 1/2W
R29 10K
R30 2.2K
R31 22K
R32 10K
C15 .001uf
R33 2.2K 1/2W
R34 10K
C16 220pf
R35 68K
R36 68K
R37 10K
C17 220pf
R38 2.2K 1/2 W
R39 10K
R40 22K
R41 22K
R42 22K
R43 22K
R44 22K
R45 22K
R46 22K
R47 47K
R48 4.7K
R49 4.7K
R50 22K
C9 220 Pf
C10 220pf
C11 220 Pf
C12 220pf
C18 220 Pf
C19 220pf
C20 220pf
C21 220 Pf
C22 220 Pf
C25 220 Pf
C26 220 Pf
C29 220 Pf
C30 220 Pf
C33 220 Pf
C39 220 Pf
CR1
CR2
CR3
CR4
CR5
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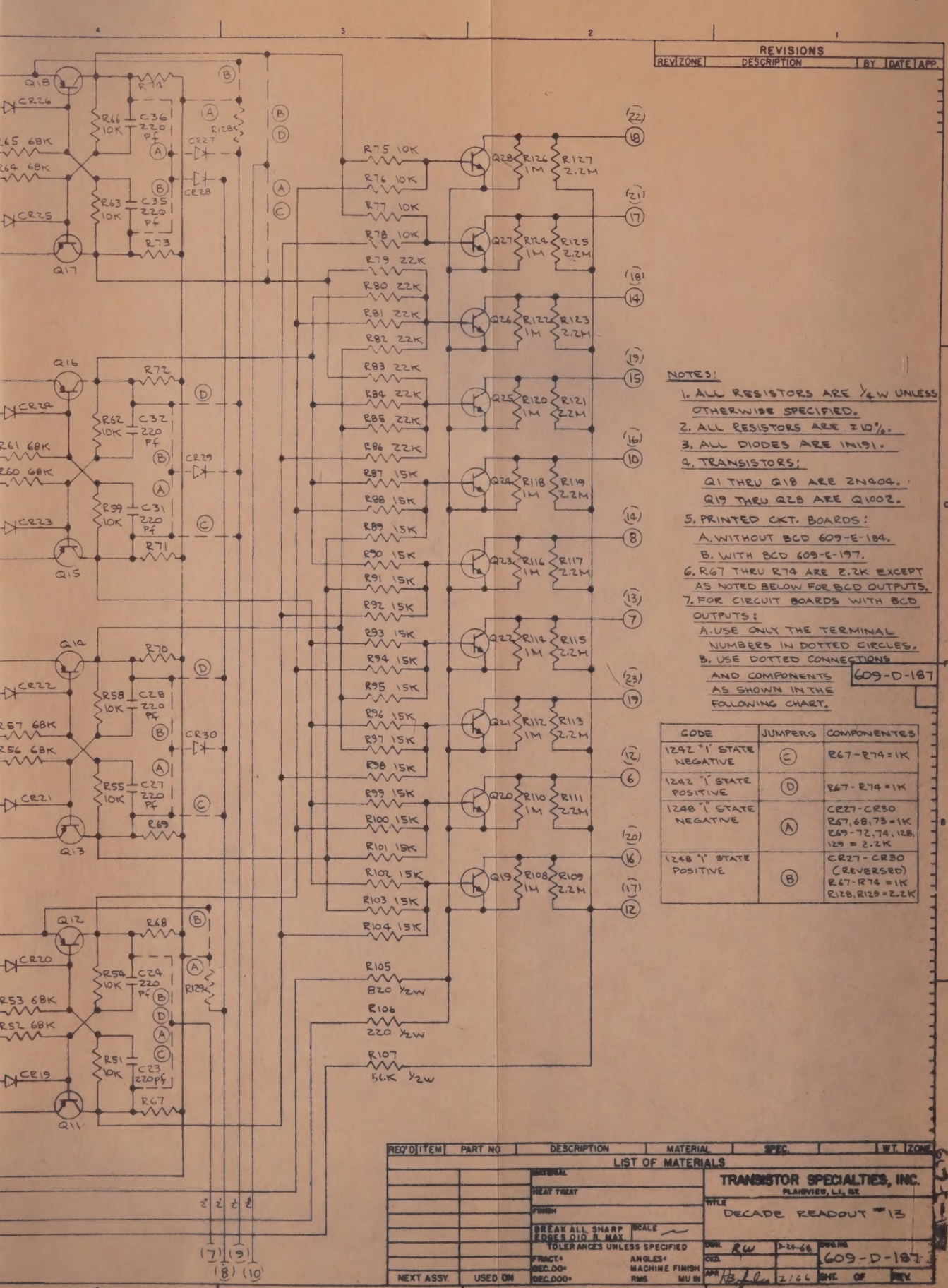
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
CR17
CR18



REVISIONS				
REV	ZONE	DESCRIPTION	BY	DATE APP

NOTES:

1. ALL RESISTORS ARE 1/2W UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE ±10%.
3. ALL DIODES ARE 1N191.
4. TRANSISTORS:
   Q1 THRU Q18 ARE 2N404.
   Q19 THRU Q28 ARE Q1002.
5. PRINTED CKT. BOARDS:
   A. WITHOUT BCD 609-E-184.
   B. WITH BCD 609-E-197.
6. R67 THRU R74 ARE 2.2K EXCEPT AS NOTED BELOW FOR BCD OUTPUTS.
7. FOR CIRCUIT BOARDS WITH BCD OUTPUTS:
   A. USE ONLY THE TERMINAL NUMBERS IN DOTTED CIRCLES.
   B. USE DOTTED CONNECTIONS AND COMPONENTS AS SHOWN IN THE FOLLOWING CHART.

609-D-187

CODE	JUMPERS	COMPONENTES
1242 "1" STATE NEGATIVE	C	R67-R74 = 1K
1242 "1" STATE POSITIVE	D	R67-R74 = 1K
1248 "1" STATE NEGATIVE	A	CR27-CR30 R67,68,73 = 1K R69-72,74,128, 129 = 2.2K
1248 "1" STATE POSITIVE	B	CR27-CR30 (REVERSED) R67-R74 = 1K R128, R129 = 2.2K

LIST OF MATERIALS

REQ'D	ITEM	PART NO	DESCRIPTION	MATERIAL	SPEC		WT.	ZONE

TRANSISTOR SPECIALTIES, INC.
PLAINVIEW, L.I., N.Y.

TITLE: DECADE READOUT #13

DWN. RW 2-24-66
CKD.
APP. 2/66

DWG. NO. 609-D-187

SHT. OF REV.

BREAK ALL SHARP EDGES .010 R. MAX.
TOLERANCES UNLESS SPECIFIED
FRACT. ± ANGLES ±
DEC. .00 ± MACHINE FINISH
DEC. .000 ± RMS MU IN

NEXT ASSY. USED ON

TRANSISTOR SPECIALTIES, INCORPORATED

www.manualsplus.com
1030865

TERMINAL DRIVE
PLAINVIEW, L. I., N. Y.
WEllis 5-8700